Titan2 series FPGA
Input and Output Interface (IO)
User Guide

(UG050006, V1.0)

(2021.06.30)

Shenzhen Ziguang Tongchuang Electronics Co., Ltd.

Document version revision record

Version number	Release date	Revision history
V0.1	2020/09/28	Initial Version
V0.2	2021/01/05	1. Update the structure diagram, source language, parameter description table and port description table of GTP_ISERDES_E2 2. Update the structure diagram, source language, parameter description table and port description table of GTP_OSERDES_E2 3. Update the effective value of the parameter of GTP_IOBUF
V0.3	2021/04/25	1. Mark which banks are HP Banks and which banks are HR Banks in Figure 2 2. Add the introduction content of IO SSN 3. Add IDDR and ODDR introduction content 4. Delete the intermediate process of the timing diagram in ISERDES and OSERDES 5. Add instructions for using BITSLIP at ISERDES 6. Instructions for adding the minimum duration of the RST signal in Table 50 and the need for synchronization of the input clock 7. Instructions for adding the minimum duration of the RST signal in Table 54 and the need for synchronization of the input clock
V1.0	2021/06/30	1. In the overview, "Titan2 series product I/O has electrostatic protection characteristics to prevent the pins of the device from being damaged by static electricity." Anti-static standards refer to the data sheet ESD 2. In the terminal matching resistance, it is stated that on-chip configurable terminal resistance can be provided for differential interface and single-ended interface 3. Delete the power supply voltage data table used by HP HR 4. Delete the level standard of non-programmable modification drive current in Table 6 and Table 7 5. Change GTP_OUTBUFCO to GTP_OUTBUFCO_E1, and modify related introduction content 6. Change GTP_OUTBUFTCO to GTP_OUTBUFTCO_E1, and modify related introduction content 7. Change GTP_IOBUFCO to GTP_IOBUFCO_E1, and modify the relevant introduction content 8. Modify the description of the port DELAY_SEL in Table 45, and introduce that the STEP value is a typical value 9. Introduce that the port RST in Table 50 is active high 10 Change "High-Speed Memory DDR 4:1 serialization mode" in Table 53 to "High-Speed Memory SDR 4:1 serialization mode, "High-Speed Memory DDR 8:1 serialization mode" to "High-Speed Memory DDR 8:1 serialization mode" -Speed Memory SDR 8:1 serialization mode 11. Introduce that the port RST in Table 54 is active high 12. Under the parameter description table of GTP_ISERDES_E2, comment on the usage instructions of HMDDR and LMDDR modes

Glossary

Abbreviations	Full Spelling
OD	Over Drive
UD	Under Drive

Table of contents

Figure catalog

Table of Contents

1. Overview of I/O unit

Document design parameters, specifications, etc. are the design goals, and the specific parameters are subject to the actual measurement data specifications of the final product.

The Titan2 family of programmable logic devices has configurable high-performance I/O drivers and receivers that support a variety of standard interfaces.

The I/O unit of Titan2 series products is mainly composed of two parts, IO BUFFER and IO LOGIC, which are generally distributed in pairs. The schematic diagram of its structure is as follows:

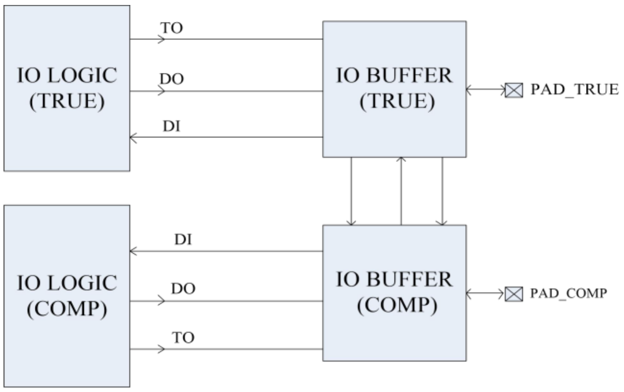


Figure 1 I/O Schematic

Each IO BUFFER will be directly connected to an IO LOGIC, which includes data input and output, and the three-state control signal of the IO BUFFER. The IO LOGIC can be configured as ISERDES or OSERDES.

The single-ended I/O standards supported by Titan2 series products include: LVCMOS, LVTTL33, SSTL, HSTL, HSUL, LPDDR, PCI33, POD12.

True differential I/O standards supported by Titan2 series products include: LVDS, Mini-LVDS, MIPI, pseudo differential standards include: RSDS, PPDS, BLVDS, TMDS, HSUL12D, SSTL12D, SSTL135D_I, SSTL135D_II, HSTL15D_I, HSTL15D_II, HSTL18D_I, HSTL18D _IILPDDRD, SSTL15D_I, SSTL15D_II, SSTL18D_I, SSTL18D_II, POD12D.

The I/O of Titan2 series products has electrostatic protection features to prevent the pins of the device from being damaged by static electricity. For anti-static standards, see "DS05001_Titan2 Series FPGA Device Data Sheet".

2. Detailed introduction of I/O unit

(1) Titan2 series I/O BANK

1. I/O BANK Distribution

The I/O of Titan2 series products are distributed according to BANK.

PG2T390H has 10 BANKs, and their distribution is shown in the figure below.

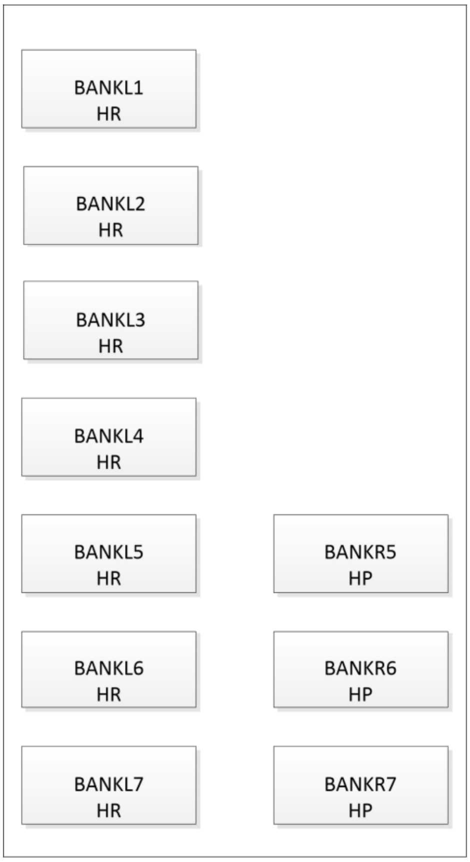


Figure 2 PG2T390H I/O BANK

BANKL1, BANKL2, BANKL3, BANKL4, BANKL5, BANKL6, BANKL7 are HRIOB, BANKR5, BANKR6, BANKR7 are HPIOB.

2. I/O BANK Voltage

Titan2 series products have certain restrictions on the I/O standards used in BANK, and the output standard voltage must match VCCIO. Titan2 products have built-in dedicated circuits to make input standards compatible with different VCCIOs. Mixed voltage LVCMOS in BANK Level standard input and output combination modes are detailed in the table below:

Table 1 Mixed Voltage LVCOMS Level Standard Input and Output Combination Modes in BANK

VCCIO (V)	Input (V)					Output (V)				
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3
1.2	√					√				
1.5		√					√			
1.8			√					√		
2.5				√					√	
3.3					√					√

Any I/O standard used in BANK, its VCCIO level must comply with the limit, Pango Design Suite software will check.

(2) IO BUFFER

Titan2 series products have configurable high-performance I/O drivers and receivers, and support a variety of input and output standards. The output drive current, slew rate, on-chip terminal resistance and other characteristics can be programmed. Each bank contains 50 IO, 2 single-ended pins, 24 pairs of differential pins. There are also two dedicated IOBs to support external reference voltage input for HSTL and SSTL input standards.

1. IO BUFFER Structure

Each IO BUFFER contains input, output and tri-state I/O drivers. These drivers can be configured into different kinds of I/O standards. There are 2 kinds of golden models for IO BUFFER.

- IOBSHR（IOBS）

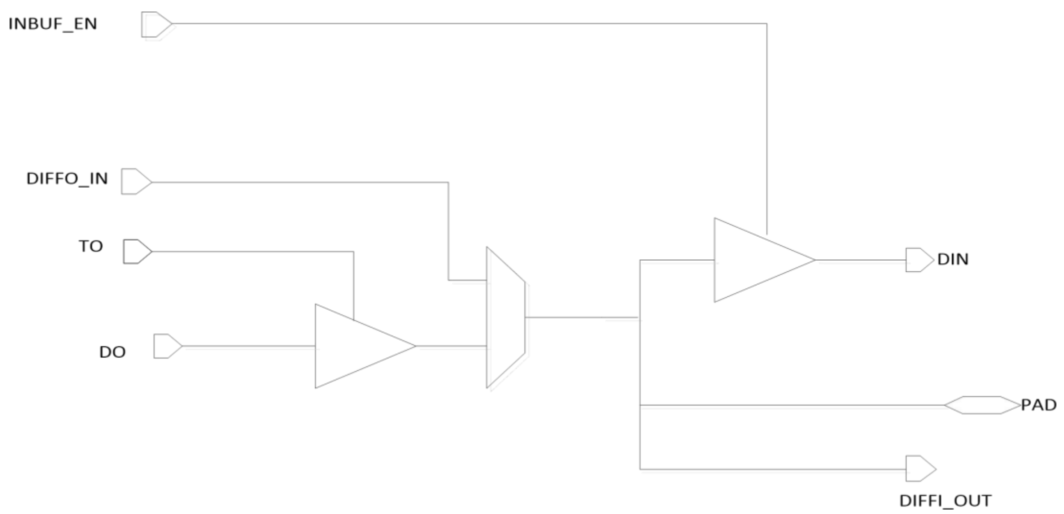


Figure3 IO BUFFER golden model (IOBSHR)

➢ IOBDHR (IOBD)

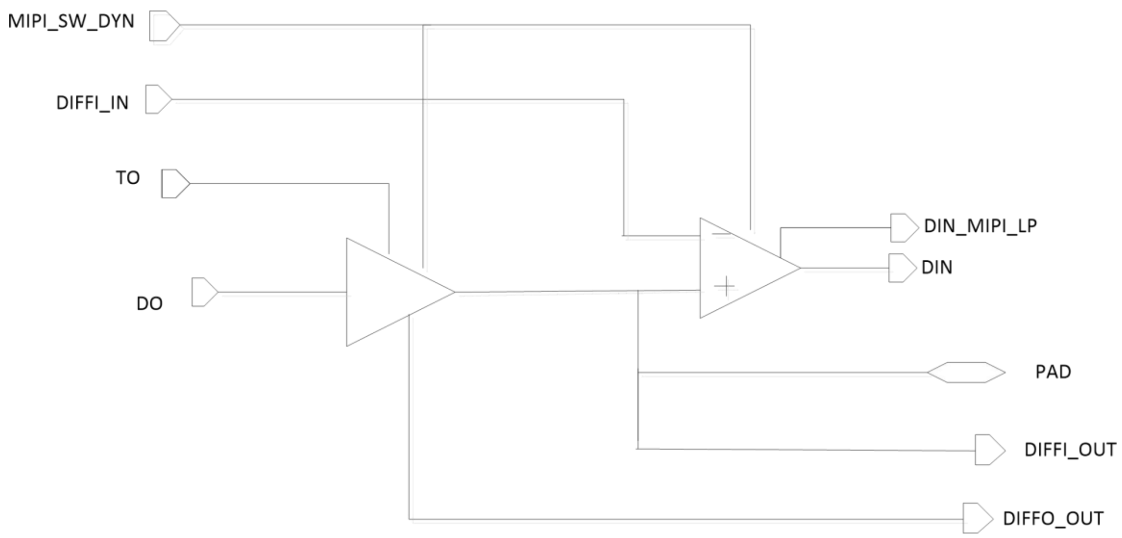


Figure 4 IO BUFFER golden model (IOBDHR)

2. Terminal matching resistance

When using high-speed I/O standards, in order to meet the signal integrity, termination resistors are usually used. The termination resistors should be as close as possible to the receiver to minimize the interference factors of signal integrity.

Titan2 series FPGAs provide on-chip configurable termination resistors for differential interfaces (such as LVDS) and single-ended interfaces (such as SSTL). If the termination resistors are configured in the IO BUFFER, the external termination resistors are not needed.

➢ Differential signal terminal matching:

The differential input uses 100Ω parallel resistors. The figure below shows the block diagram of the external and internal termination resistors.

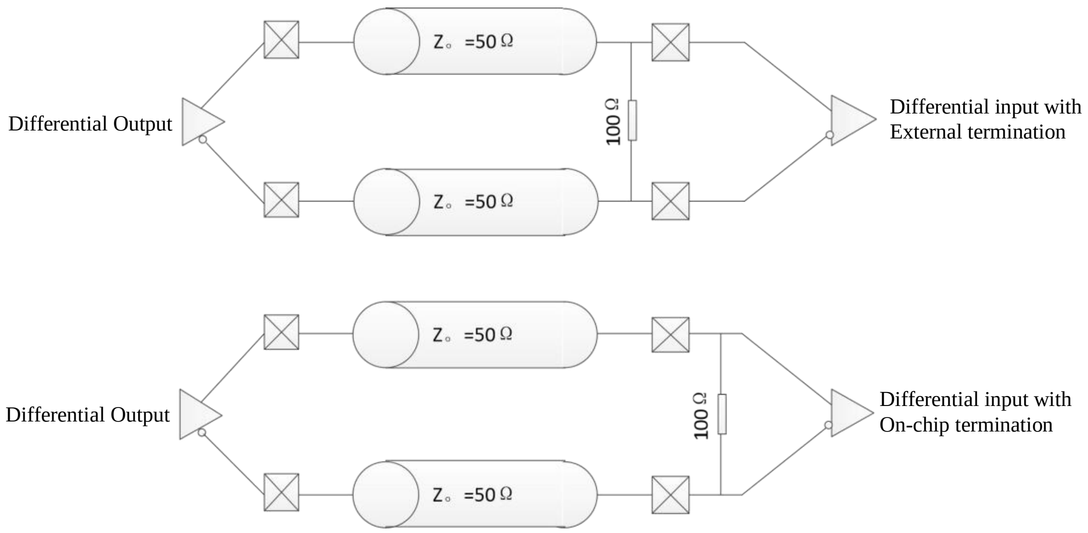
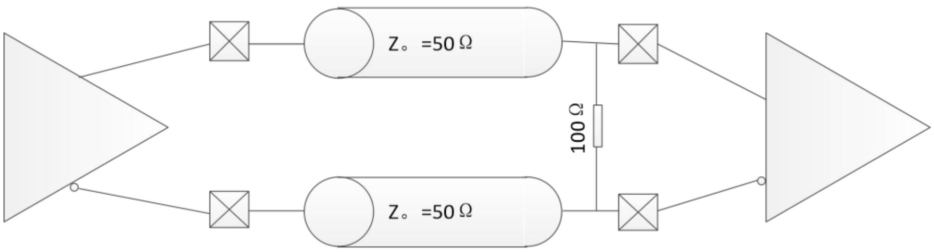


Figure 5 Matching resistors for chip differential signals

The optional on-chip differential termination of Titan2 series FPGA can eliminate the 100Ω external termination resistor. This kind of on-chip differential termination resistor does not need to be adjusted and is fully applicable to LVDS, MIPI level standards.

Optional on-chip differential termination is configurable through I/O constraints. Figure 6 shows different implementations using on-chip differential termination at the differential receiver side or with external termination resistors.

a. The differential pair uses an external termination resistor, constraining DIFF_IN_TERM_MODE=OFF



b. Differential pair on-chip differential terminal, constrain DIFF_IN_TERM_MODE=ON

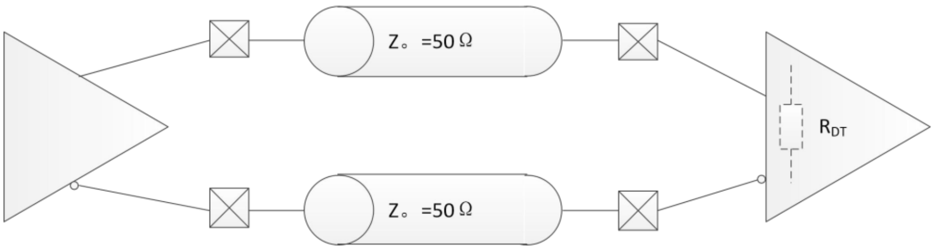


Figure 6 Selection method of terminal resistance at differential input

When the attribute DIFF_IN_TERM_MODE of the I/O pin is set to "ON", the on-chip differential termination is enabled. When constraining in the FDC file, use the following command:

```
define_attribute {p:port_name} {PAP_IO_DIFF_IN_TERM_MODE} {ON}
```

- Single-ended signal termination:

Single-ended signal termination supports SSTL, HSTL and POD interfaces. For storage interfaces, the matching resistors are as follows:

Interface Type	LPDDR	DDR2	DDR3	DDR4
HP BANK Matching resistance	60/40ohm	60/40ohm	60/40ohm	240/120/80/60/48/40/34ohm
HR BANK Matching resistance	60/50/40ohm	60/50/40ohm	60/50/40ohm	-

Note: For the HP BANK ddr memory interface, a 240-ohm matching resistor needs to be connected in series to the ground on the VRP pin, and the other VRN can be used as a normal IO.

Figure 7 is a schematic diagram of the internal termination of SSTL and HSTL, for HR BANK, R1, R2 are 80/100/120 ohms, for HP BANK, R1, R2 are 80/120 ohms.

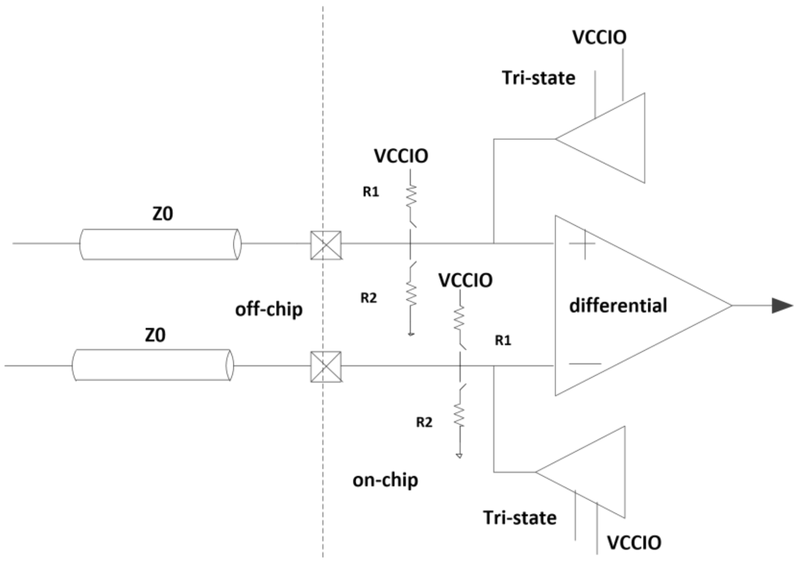


Figure 7 SSTL, HSTL internal resistance termination method

In the FDC file, on-chip termination can be enabled through I/O constraints. The constraints are as follows:

```
define_attribute { p:port_name } {PAP_IO_DDR_TERM_MODE} {ON}
```

Among them, if you want to enable the on-chip terminal, select the parameter "ON"; otherwise, select "OFF".

3. Supported I/O Standards

The IO BUFFER of Titan2 series programmable logic devices supports a wide range of single-ended I/O signal standards, and all I/Os can be used to form differential pairs, which can support many differential signal standards. This flexibility can make the user selects the most appropriate I/O standard for each pin to meet the needs of interface and signal integrity. These I/Os are allocated in several independent BANKs, and each BANK has a common output voltage (VCCIO) inside and a common reference voltage (VREF).

The trend of today's bus applications is usually led by the largest and most influential companies in the digital electronics industry. Every time they launch a bus, they will launch the corresponding I/O standard. These bus I/O standards are for those who use it the merchants who come to design products provide detailed instructions. Each I/O standard has its specific electrical performance: including current, voltage, IO Buffering and terminal technology. Titan2 series programmable logic devices follow this trend and can support continuously expanding I/O standards can be flexibly and quickly adapted to market needs. By configuring IO BUFFER drivers, I/O can support multiple I/O standards. The single-ended I/O standards supported by Titan2 series are shown in Table 2 below and Table 3:

Table 2 Standards supported by Titan2 series HR BANK

Single-ended I/O standard	Slew Rate	VCCIO	IN/OUT	Full HR BANK support
PCI33	FAST/SLOW	3.3	IN/OUT	Yes
LVTTL33	FAST/SLOW	3.3	IN/OUT/INOUT	Yes
LVCMOS33	FAST/SLOW	3.3	IN/OUT/INOUT	Yes
LVCMOS25	FAST/SLOW	2.5	IN/OUT/INOUT	Yes

Single-ended I/O standard	Slew Rate	VCCIO	IN/OUT	Full HR BANK support
LVCMOS18	FAST/SLOW	1.8	IN/OUT/INOUT	Yes
LVCMOS15	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
LVCMOS12	FAST/SLOW	1.2	IN/OUT/INOUT	Yes
HSTL15_I	FAST/SLOW	1.5	IN/OUT	Yes
HSTL18_I	FAST/SLOW	1.8	IN/OUT	Yes
HSTL15_II	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
HSTL18_II	FAST/SLOW	1.8	IN/OUT/INOUT	Yes
SSTL135_I	FAST/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL135_II	FAST/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL15_I	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
SSTL15_II	FAST/SLOW	1.5	IN/OUT/INOUT	Yes
SSTL18_I	FAST/SLOW	1.8	IN/OUT	Yes
SSTL18_II	FAST/SLOW	1.8	IN/OUT/INOUT	Yes
HSUL12	FAST/SLOW	1.2	IN/OUT/INOUT	Yes
LPDDR	FAST/SLOW	1.8	IN/OUT/INOUT	Yes

Table 3 Standards Supported by Titan2 Series HP BANK

Single-ended I/O standard	Slew Rate	VCCIO	IN/OUT	Full HP BANK support
LVCMOS12	FAST/MEDIUW/SLOW	1.2	IN/OUT/INOUT	Yes
LVCMOS15	FAST/MEDIUW/SLOW	1.5	IN/OUT/INOUT	Yes
LVCMOS18	FAST/MEDIUW/SLOW	1.8	IN/OUT/INOUT	Yes
HSTL12_I	FAST/MEDIUW/SLOW	1.2	IN/OUT	Yes
HSTL15_I	FAST/MEDIUW/SLOW	1.5	IN/OUT	Yes
HSTL18_I	FAST/MEDIUW/SLOW	1.8	IN/OUT	Yes
HSTL15_II	FAST/MEDIUW/SLOW	1.5	IN/OUT/INOUT	Yes
HSTL18_II	FAST/MEDIUW/SLOW	1.8	IN/OUT/INOUT	Yes
SSTL18_I	FAST/MEDIUW/SLOW	1.8	IN/OUT	Yes
SSTL18_II	FAST/MEDIUW/SLOW	1.8	IN/OUT/INOUT	Yes
SSTL15_I	FAST/MEDIUW/SLOW	1.5	IN/OUT	Yes
SSTL15_II	FAST/MEDIUW/SLOW	1.5	IN/OUT/INOUT	Yes
SSTL135_I	FAST/MEDIUW/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL135_II	FAST/MEDIUW/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL12	FAST/MEDIUW/SLOW	1.2	IN/OUT/INOUT	Yes
HSUL12	FAST/MEDIUW/SLOW	1.2	IN/OUT/INOUT	Yes
POD12	FAST/MEDIUW/SLOW	1.2	IN/OUT/INOUT	Yes
POD12_CAL	FAST/MEDIUW/SLOW	1.2	IN/OUT/INOUT	Yes
HSTL15_I_CAL	FAST/MEDIUW/SLOW	1.5	IN/OUT	Yes
HSTL18_I_CAL	FAST/MEDIUW/SLOW	1.8	IN/OUT	Yes
HSTL15_II_CAL	FAST/MEDIUW/SLOW	1.5	IN/OUT/INOUT	Yes
HSTL18_II_CAL	FAST/MEDIUW/SLOW	1.8	IN/OUT/INOUT	Yes
SSTL18_I_CAL	FAST/MEDIUW/SLOW	1.8	IN/OUT	Yes
SSTL18_II_CAL	FAST/MEDIUW/SLOW	1.8	IN/OUT/INOUT	Yes
SSTL15_I_CAL	FAST/MEDIUW/SLOW	1.5	IN/OUT	Yes

Single-ended I/O standard	Slew Rate	VCCIO	IN/OUT	Full HP BANK support
SSTL15_II_CAL	FAST/MEDIUW/SLOW	1.5	IN/OUT/INOUT	Yes
SSTL135_I_CAL	FAST/MEDIUW/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL135_II_CAL	FAST/MEDIUW/SLOW	1.35	IN/OUT/INOUT	Yes
SSTL12_CAL	FAST/MEDIUW/SLOW	1.2	IN/OUT/INOUT	Yes
HSUL12_CAL	FAST/MEDIUW/SLOW	1.2	IN/OUT/INOUT	Yes
LVCAL_15	FAST/MEDIUW/SLOW	1.5	IN/OUT/INOUT	Yes
LVCAL_18	FAST/MEDIUW/SLOW	1.8	IN/OUT/INOUT	Yes
HSLVCAL_15	FAST/MEDIUW/SLOW	1.5	IN/OUT/INOUT	Yes
HSLVCAL_18	FAST/MEDIUW/SLOW	1.8	IN/OUT/INOUT	Yes

Description: Level standard with CAL has resistance calibration function

LVTTL33 (Low-Voltage TTL): 3.3V standard defined by JESD, 3.3V VCCIO is required for output, no reference voltage and termination voltage are required.

LVCMOS (Low-Voltage CMOS): Low-voltage CMOS standard, the application voltage ranges from 1.2V to 3.3V. No reference voltage and termination voltage are required.

SSTL18 (Stub Series Terminated Logic for 1.8V): Defined by JESD79-2C, 1.8V memory bus standard. Requires 0.90V reference voltage, 1.8V VCCIO and a 0.90V termination voltage. SSTL18 is used for high-speed SDRAM interface.

SSTL15 (Stub Series Terminated Logic for 1.5V): Defined by JESD79-3, 1.5V memory bus standard. Requires 0.75V reference voltage, 1.5V VCCIO and a 0.75V termination voltage. SSTL15 is used for high-speed SDRAM interface.

SSTL135 (Stub Series Terminated Logic for 1.35V): Defined by JESD79-3-1, 1.35V memory bus standard. Requires 0.675V reference voltage, 1.35V VCCIO and a 0.675V termination voltage. SSTL135 is used for DDR3L SDRAM storage interface.

HSTL18 (High-Speed Transceiver Logic for 1.8V): Defined by IBM, a high-speed bus standard. It requires a reference voltage of 0.90V, a VCCIO of 1.8V and a termination voltage of 0.90V.

HSTL15 (High-Speed Transceiver Logic for 1.5V): Defined by IBM, a high-speed bus standard. It requires a reference voltage of 0.75V, a VCCIO of 1.5V and a termination voltage of 0.75V.

HSUL12 (High-Speed Unterminated Logic for 1.2V): Defined by JESD8-22B, a high-speed bus standard. It requires a reference voltage of 0.6V, a VCCIO of 1.2V and a termination voltage of 0.6V. HSUL12 is used to improve high-speed data transmission bus power consumption.

The differential output of Titan2 series products is divided into two types: true differential output and quasi-differential output:

The true differential output is supported by a dedicated circuit with high performance, including LVDS_18, LVDS25, RSDS, MINI-LVDS, PPDS, TMDS. Differential pairs in the Titan2 series all support true differential output.

The class differential output is realized on the basis of the LVCMOS output standard combined with the external resistance of the chip. The combination of COMP PAD and TRUE PAD driven by a single end is the complementary output mode. The class differential output mode is used to drive the complementary SSTL standard, HSTL standard, HSUL standard and BLVDS.

The differential I/O standards supported by the Titan2 series are listed in the table below:

Table 4 Differential I/O Standards Supported by Titan2 Series HR BANK

Differential I/O Standards	VCCIO (V)		IN/OUT	Note	Full HR BANK support
	Output	Input			
LVDS25	2.5	1.8/2.5/3.3	IN/OUT	All banks support LVDS true differential output, with internal termination resistor	Yes
RSDS	2.5	2.5	IN/OUT	With internal termination resistor	Yes
MINI-LVDS	2.5	2.5	IN/OUT	With internal termination resistor	Yes
PPDS	2.5	2.5	IN/OUT	With internal termination resistor	Yes
TMDS	3.3	3.3	IN/OUT	Open drain connection	Yes
BLVDS	2.5	2.5	IN/OUT/INOUT	Bidirectional multi-point drive input and output differential signals. The output is supported by a class differential method combined with external resistors. The input is connected in a differential manner	Yes
SSTL18D_I	1.8	1.8	IN/OUT	The output is implemented in a differential-like manner	Yes
SSTL18D_II	1.8	1.8	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL15D_I	1.5	1.5	IN/OUT	The output is implemented in a differential-like manner	Yes
SSTL15D_II	1.5	1.5	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSTL18D_I	1.8	1.8	IN/OUT	The output is implemented in a differential-like manner	Yes
HSTL18D_II	1.8	1.8	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSTL15D_I	1.5	1.5	IN/OUT	The output is implemented in a differential-like manner	Yes
HSTL15D_II	1.5	1.5	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSUL12D	1.2	1.2	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes

Table 5 Differential I/O Standards Supported by Titan2 Series HP BANK

Differential I/O Standards	VCCIO (V)		IN/OUT	Note	Full HR BANK support
	Output	Input			
LVDS_18	1.8	1.8	IN/OUT	With internal termination resistor	Yes
MIPI	1.2	1.2	IN/OUT	With internal termination resistor	Yes
SSTL18D_I	1.8	1.8	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL18D_II	1.8	1.8	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL15D_I	1.5	1.5	IN/OUT	The output is implemented in a differential-like manner	Yes
SSTL15D_II	1.5	1.5	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL135D_I	1.35	1.35	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL135D_II	1.35	1.35	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL12D	1.2	1.2	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSTL18D_I	1.8	1.8	IN/OUT	The output is implemented in a differential-like manner	Yes
HSTL18D_II	1.8	1.8	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSTL15D_I	1.5	1.5	IN/OUT	The output is implemented in a differential-like manner	Yes
HSTL15D_II	1.5	1.5	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSTL12D_I	1.2	1.2	IN/OUT	The output is implemented in a differential-like manner	Yes
HSUL12D	1.2	1.2	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
POD12D	1.2	1.2	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL18D_I_CAL	1.8	1.8	IN/OUT	The output is implemented in a differential-like manner	Yes
SSTL18D_II_CAL	1.8	1.8	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes

Differential I/O Standards	VCCIO (V)		IN/OUT	Note	Full HR BANK support
	Output	Input			
SSTL15D_I_CAL	1.5	1.5	IN/OUT	The output is implemented in a differential-like manner	Yes
SSTL15D_II_CAL	1.5	1.5	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL135D_I_CAL	1.35	1.35	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL135D_II_CAL	1.35	1.35	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
SSTL12D_CAL	1.2	1.2	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSTL18D_I_CAL	1.8	1.8	IN/OUT	The output is implemented in a differential-like manner	Yes
HSTL18D_II_CAL	1.8	1.8	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSTL15D_I_CAL	1.5	1.5	IN/OUT	The output is implemented in a differential-like manner	Yes
HSTL15D_II_CAL	1.5	1.5	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
HSUL12D_CAL	1.2	1.2	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes
POD12D_CAL	1.2	1.2	IN/OUT/INOUT	The output is implemented in a differential-like manner	Yes

Description: Level standard with CAL has resistance calibration function

LVDS25 (Low Voltage Differential Signal): Differential standard, one data bit is transmitted through two signal lines, so it has inherent immunity to noise compared to single-ended I/O standards. The voltage swing between the two signal lines about 350mV. There is no need for reference voltage and termination voltage. The LVDS input terminal needs matching resistors. You can use discrete resistors on the PCB, or you can use the DIFF_IN_TERM_MODE attribute to enable the chip's internal terminal matching resistors.

RSDS (Reduced Swing Differential Signaling): A panel internal (intra-panel) bus interface standard, usually used in the display field. It defines the emission, reception characteristics and protocol of the chip-chip interface. RSDS input requires parallel termination resistors, you can use a discrete resistor on the PCB, or you can use the DIFF_IN_TERM_MODE attribute to enable the chip's internal terminal matching resistor.

MINI-LVDS is developed based on the LVDS interface standard. It is usually used in the field of flat panel display as the interface between the timing control module and the LCD. It has a smaller swing, generates very low electromagnetic interference, and can drive the display Provides high bandwidth.

PPDS (Point-to-Point Differential Signaling): The next-generation LCD internal display interface standard. PPDS input requires parallel termination resistors, which can be discrete resistors on the PCB, or enable chip internal termination matching resistors through the DIFF_IN_TERM_MODE attribute.

TMDS (Transition Minimized Differential Signaling): Over-modulated differential signal, also known as minimized transmission differential signal, applied to DVI, HDMI interface.

BLVDS (Bus Low Voltage Differential Signaling): It is an output standard similar to the MLVDS standard proposed by NS (National Semiconductor), and it is also used as a case where bidirectional multi-point drive output input differential signals are required. The difference between the two is that, MLVDS is an industry standard. The differential amplitude of MLVDS is larger than that of BLVDS, and requires a higher current drive capability. I/O itself does not support BLVDS, and it needs to be realized with the complementary output principle of LVCMOS and external resistors on the chip. SSTL18D, SSTL15D, HSTL18D, HSTL15D, HSUL12D, POD12D and other differential outputs are implemented in a differential-like manner.

Different I/O standards have different timings. The Pango Design Suite software tool will analyze the Timing timing of I/O, and the timing analysis report will include this information.

The I/O standard can be constrained in the FDC file or operated in the UCE interface of PDS by the following statement.

```
define_attribute {p:port_name} {PAP_IO_STANDARD} { LVCMOS33 }
```

4. I/O Supply Voltage Introduction

According to the actual user design, the IO BUFFER is powered by a mixture of three main power supplies of the FPGA, which are VCC, VCCA and VCCIO. For the power supply voltage data, please refer to the "DS05001_Titan2 Series FPGA Device Data Sheet".

- VCC

VCC is the core voltage of HR BANK, which is mainly used to supply power to the control logic circuit of IO BUFFER and most of the circuits of IO LOGIC. When outputting data from the core, the control signal passes through the control logic of IO LOGIC and IO BUFFER so that the data signal is transmitted by The VCC power supply is converted to a higher power supply voltage; when inputting data to the core, the control signal passes through the control logic of the IO BUFFER and the IO LOGIC so that the data signal is converted from a high power supply voltage to a VCC power supply.

- VCCA

VCCA is the auxiliary power supply voltage, which is mainly used to power the differential output drive circuit, differential input circuit and input circuit with reference voltage applied in SSTL standard and HSTL standard.

- VCCIO

The VCCIO voltage is independently powered in each BANK, mainly for the single-ended output drive circuit and the ratio input circuit. Therefore, the characteristic values of the input and output standards powered by the VCCIO power supply will change with the VCCIO power supply voltage.

- VCC_HP

VCC_HP is the HP BANK core power supply voltage.

- VCCA_IO

VCCA_IO is the auxiliary power supply voltage of HP BANK, mainly used for differential output drive circuit

- GND

Although inside the I/O circuit, different power supply voltages may correspond to different grounds for layout planning and signal division, for example, VCCIO corresponds to VSSIO, VCCA corresponds to VSS, VCC corresponds to VSS, etc. But at the top level of the chip, all These I/O grounds are all connected to a common GND during the packaging process.

5. BUS KEEPER Feature

The main function of the BUS KEEPER circuit is to keep the current I/O data state until the next I/O data is valid. Each I/O has an independent BUS KEEPER function, usually with four programmable working modes, PULLUP, PULLDW, KPR and NONE. The BUS KEEPER feature can be edited in the FDC file or operated in the UCE of the PDS through the following statement.

```
define_attribute {p:port_name} {PAP_IO_NONE} {TRUE}
```

6. Input Hysteresis Characteristics

LVCMOS33/LVTTL33/LVCMO25/LVCMOS18/ LVCMOS15/ LVCMOS12 input standards can support input hysteresis characteristics. The input hysteresis characteristics can be edited in the FDC file by the following statement or operated in the UCE of PDS.

```
define_attribute {p:port_name} {PAP_IO_HYS_DRIVE_MODE} {NOHYS}
```

7. IO port status

During power-on, all IOs including user IOs, multiplexed IO output buffers are disabled and are in a high-impedance state.

After the power-on process is over, during the initialization process and programming process, the multiplexed IO pin IO_STATUS_C is used to control the port status of all user IOs. When the IO_STATUS_C input is low, the internal weak pull-up of the IO will be enabled. When the IO_STATUS_C input is High level, will disable IO internal weak pull-up, IO output high-impedance state.

Enter the user mode after the programming process is over, and the user logic controls the input and output mode and port status of the user IO. If persist="on", the multiplexed IO is still used for configuration, if persist="off", the multiplexed IO is used for user IO.

8. Input Buffer

Each pin of the input terminal has two types of input buffers to meet the requirements of different input standards. The first type is LVCMOS single-ended buffer with power supply voltage VCCIO; the second type is input buffer with power supply voltage VCCA. The class input buffer can realize the input standard and differential input standard whose reference voltage determines the threshold.

9. Buffer Reference Voltage VREF

Input and output standards with a reference voltage, such as SSTL and HSTL standards, require a reference voltage to set the threshold. The reference voltage can be generated in two ways. The first way is to input an external test voltage through the I/O pin; the second the first method can be generated by the internal reference voltage generation circuit of the chip. In the first method, there are 2 dedicated I/Os in each BANK used as the input of the external VREF. In the second method, the reference voltage is generated by the chip internal the reference voltage generation circuit provides VREF reference voltage for all I/Os in the entire BANK to support the input and output standards that require a reference voltage. Each BANK will correspond to an internal reference voltage generation circuit, and the output of the reference voltage can be set by programming. The two methods of generating VREF reference voltage need to be set and selected through programming. As a dedicated IO for VREF input, if it is not used as a VREF pin, it can be used as a normal IO.

Use the following statement to make constraints in the FDC file, or operate in the UCE interface of PDS.

```
define_attribute {p:port_name} {PAP_IO_VREF_MODE_VALUE} {0.5}
```

10. Programmable output drive capability

Table 6 HR BANK IO programmable output drive capability

IO standard	driver strength
LVTTL33	4mA, 8mA, 12mA, 16mA, 24mA
LVCMOS33/25	4mA, 8mA, 12mA, 16mA
LVCMOS18	4mA, 8mA, 12mA, 16mA, 24mA
LVCMOS15	4mA, 8mA, 12mA, 16mA
LVCMOS12	4mA, 8mA, 12mA
LVDS25	3mA, 3.5mA, 4.0mA, 4.5mA
RSDS	
MINI-LVDS	3mA, 4.0mA, 4.5mA, 5mA
PPDS	2mA, 2.5mA, 3mA, 3.5mA
TMDS	4.5mA, 5mA
BLVDS	4mA, 8mA, 12mA, 16mA

Table 7 HP BANK IO Programmable Output Drive Capabilities

IO standard	driver strength
LVCMOS18	2mA, 4mA, 6mA, 8mA, 12mA, 16mA
LVCMOS15	2mA, 4mA, 6mA, 8mA, 12mA, 16mA
LVCMOS12	2mA, 4mA, 6mA, 8mA
LVDS_18	3mA, 3.5mA, 4.0mA, 4.5mA

11. Open-Drain Control

The single-ended output driver circuit of each IOB can independently support the Open-Drain function. That is, when the Open-Drain is output, the output driver circuit only includes the sink part, and does not provide the source current.

The control of Open-Drain includes opening and closing, that is, ON and OFF. The control of Open-Drain can be constrained in the FDC file through the following statement, or constrained in the UCE interface of PDS.

```
define_attribute {p:port_name} {PAP_IO_OPEN_DRAIN} {OFF}
```

12. Three-state control output

For IO BANK, in the output path of I/O, each single-ended output drive circuit has an independent three-state control circuit. In addition, a flag signal IO_STATUS_C is generated through a multiplexed I/O to control the port status of all I/O in the configuration process. When IO_STATUS_C=0, it means that the I/O of the configuration process is in three states; when IO_STATUS_C=1, it means that the I/O of the configuration process is in pull-up. The three-state control of the differential drive circuit adopts the three-state control of the single-ended output drive of TRUE pad.

13. Programmable slew rate

According to the requirements of reducing output noise or improving high-speed output performance, the output driver of each I/O has a programmable slew rate control setting, which is used to provide output slew rate control for the output. The slew of each I/O The rate control is independent. The parameters that can be set for HR BANK IO are: "FAST" and "SLOW". The parameters that can be set for HP BANK IO are: "FAST", "MEDIUW" and "SLOW".

The programmable slew rate can be constrained in the FDC file by the following statement, or constrained in the UCE interface of PDS.

```
define_attribute { p:port_name } {PAP_IO_SLEW} {FAST}
```

14. Class Differential Output Implementations

The BLVDS output buffer does not adopt the LVDS differential structure, but uses two LVCMOS single-ended output buffers plus an external resistor connection to realize the BLVDS output interface level.

➢ Class differential output – BLVDS

BLVDS is an output standard similar to the MLVDS standard proposed by NS (National Semiconductor), and it is also used as a situation where bidirectional multi-point drive output and input differential signals are required. The difference between the two is that MLVDS is an industry standard, and MLVDS's the differential amplitude is larger than that of BLVDS, and requires a higher current drive capability. I/O itself does not support BLVDS, and still needs to be implemented with the complementary output principle of LVCMOS and external resistors on the chip. The figure below shows the multi-point configuration of BLVDS the typical application situation. Among them, R0 and R1 should be based on the perspective of circuit design and verification, and the reference value should be given under the condition of ensuring that the output level meets the standard requirements. R1=80 ohms, R1=40~100 ohms, the exact specific values It depends on the actual chip test results given by the final product engineer.

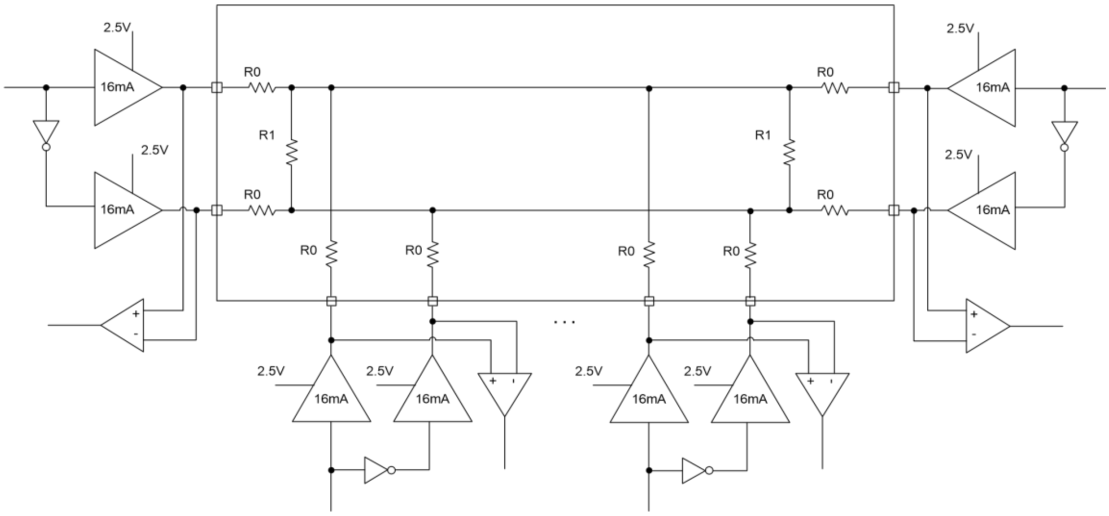
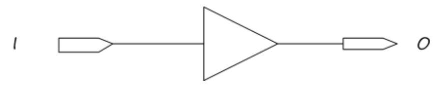
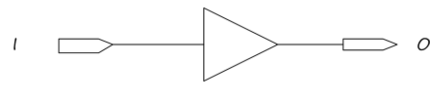
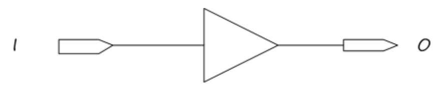
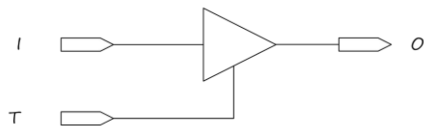
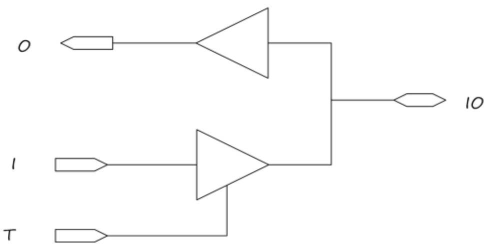


Figure 8 Example of BLVDS point-to-point output

15. IO BUFFER's GTP basic prototype

The software library of Pango Design Suite contains related GTP (General Technology Primitives) to support various I/O standards. The following GTP basic prototypes are the most common in single-ended I/O standards, and more GTP See "UG050007_Titan2 Series GTP User Guide".

Table 8 GTP for single-ended I/O

GTP Name	GTP Description	GTP schematic diagram
GTP_INBUF	Single-ended input signal must go through INBUF, support IOBD, IOBS	
GTP_INBUFG	INBUFG Same as INBUF, input signal for clock input pin	
GTP_OUTBUF	Support single-ended output signal	
GTP_OUTBUFT	Used to achieve three-state output	
GTP_IOBUF	Support single-ended input and output functions	

- GTP_INBUF

Port descriptions are as follows:

Table 9 GTP_INBUF port description

Port	Direction	Functional description
I	IN	Single-ended signal input
O	OUT	Input buffer output, sent to the chip

The parameter description is as follows:

Table 10 GTP_INBUF parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	See Table 11	"LVCMOS33"	Input IO standard
TERM_DDR	string	See Table 11	"ON"	HSTL, SSTL standard input, the built-in termination resistor is on or off

The optional configuration properties for parameters are as follows:

Table 11 Parameter configuration list

GTP_INBUF	
IOSTANDARD	TERM_DDR
LVTTL33	None
PCI33	
LVCMOS33	
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL25_I	OFF/ON
SSTL25_II	OFF/ON
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I_CAL	ON
SSTL15_II_CAL	ON
HSTL15_I_CAL	ON
SSTL135_I	OFF/ON
SSTL135_II	OFF/ON
SSTL12	OFF/ON
HSTL12_I	OFF/ON
HSUL12	OFF/ON
POD12	OFF/ON
HSTL15_II	OFF/ON
SSTL18_I_CAL	ON
SSTL18_II_CAL	ON
SSTL15_I_CAL	ON
SSTL15_II_CAL	ON
HSTL18_I_CAL	ON
HSTL18_II_CAL	ON
HSTL15_I_CAL	ON
HSTL15_II_CAL	ON
SSTL135_I_CAL	ON
SSTL135_II_CAL	ON
SSTL12_CAL	ON

GTP_INBUF	
IOSTANDARD	TERM_DDR
HSTL12_I_CAL	ON
HSUL12_CAL	ON
POD12_CAL	ON
LVCAL_15	None
LVCAL_18	
HSLVCAL_15	
HSLVCAL_18	

- GTP_INBUFG

Port descriptions are as follows:

Table 12 GTP_INBUFG port description

Port	Direction	Functional description
I	IN	PAD signal input
O	OUT	Buffer output, sent to the chip

The parameter description is as follows:

Table 13 GTP_INBUFG parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	See Table 14	"LVCMOS33"	Input IO standard
TERM_DDR	string	See Table 14	"ON"	HSTL, SSTL standard input, the built-in terminal resistor is enabled or disabled

The list of valid values for parameter configuration is as follows:

Table 14 List of valid values of parameters

GTP_INBUFG	
IOSTANDARD	TERM_DDR
LVCMOS33	None
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL25_I	OFF/ON
SSTL25_II	OFF/ON
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I_CAL	ON
SSTL15_II_CAL	ON
HSTL15_I_CAL	ON
SSTL135_I	OFF/ON
SSTL135_II	OFF/ON

GTP_INBUFG	
IOSTANDARD	TERM_DDR
SSTL12	OFF/ON
HSTL12_I	OFF/ON
HSUL12	OFF/ON
POD12	OFF/ON
HSTL15_II	OFF/ON
SSTL18_I_CAL	ON
SSTL18_II_CAL	ON
HSTL18_I_CAL	ON
HSTL18_II_CAL	ON
HSTL15_II_CAL	ON
SSTL135_I_CAL	ON
SSTL135_II_CAL	ON
SSTL12_CAL	ON
HSTL12_I_CAL	ON
HSUL12_CAL	ON
POD12_CAL	ON
LVCAL_15	None
LVCAL_18	
HSLVCAL_15	
HSLVCAL_18	

- GTP_OUTBUF

Port descriptions are as follows:

Table 15 GTP_OUTBUF port description

Port	Direction	Functional description
I	IN	Single-ended signal input
O	OUT	buffer output

The parameter description is as follows:

Table 16 GTP_OUTBUF parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	See Table 17	"LVCMOS33"	Input IO standard
SLEW_RATE	string	"SLOW","MEDIUM", "FAST"	"SLOW"	Slew rate
DRIVE_STRENGTH	string	"2", "4", "6", "8", "12", "16", "24"	"8"	Drive current strength

The list of valid values for the parameters is as follows:

Table 17 List of valid values of parameters

GTP_OUTBUF		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
LVTTTL	FAST/SLOW	"4", "8", "12", "16", "24"
PCI33	None	None
LVCMOS33	FAST/SLOW	"4", "8", "12", "16"
LVCMOS25	FAST/SLOW	"4", "8", "12", "16"
LVCMOS18	FAST/SLOW/MEDIUM	"2", "4", "6", "8", "12", "16", "24"

GTP_OUTBUF		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
LVCMOS15	FAST/SLOW/MEDIUM	"2", "4", "6", "8", "12", "16"
LVCMOS12	FAST/SLOW/MEDIUM	"2", "4", "6", "8"
SSTL18_I	FAST/SLOW/MEDIUM	None
SSTL18_II	FAST/SLOW/MEDIUM	None
SSTL15_I	FAST/SLOW/MEDIUM	None
SSTL15_II	FAST/SLOW/MEDIUM	None
SSTL135_I	FAST/SLOW/MEDIUM	None
SSTL135_II	FAST/SLOW/MEDIUM	None
SSTL12	FAST/SLOW/MEDIUM	None
HSTL18_I	FAST/SLOW/MEDIUM	None
HSTL18_II	FAST/SLOW/MEDIUM	None
HSTL15_I	FAST/SLOW/MEDIUM	None
HSTL15_II	FAST/SLOW/MEDIUM	None
HSTL12_I	FAST/SLOW/MEDIUM	None
HSUL12	FAST/SLOW/MEDIUM	None
POD12	FAST/SLOW/MEDIUM	None
SSTL18_I_CAL	FAST/SLOW/MEDIUM	None
SSTL18_II_CAL	FAST/SLOW/MEDIUM	None
SSTL15_I_CAL	FAST/SLOW/MEDIUM	None
SSTL15_II_CAL	FAST/SLOW/MEDIUM	None
SSTL135_I_CAL	FAST/SLOW/MEDIUM	None
SSTL135_II_CAL	FAST/SLOW/MEDIUM	None
SSTL12_CAL	FAST/SLOW/MEDIUM	None
HSTL18_I_CAL	FAST/SLOW/MEDIUM	None
HSTL18_II_CAL	FAST/SLOW/MEDIUM	None
HSTL15_I_CAL	FAST/SLOW/MEDIUM	None
HSTL15_II_CAL	FAST/SLOW/MEDIUM	None
HSTL12_I_CAL	FAST/SLOW/MEDIUM	None
HSUL12_CAL	FAST/SLOW/MEDIUM	None
POD12_CAL	FAST/SLOW/MEDIUM	None
LVCAL_15	FAST/SLOW/MEDIUM	None
LVCAL_18	FAST/SLOW/MEDIUM	None
HSLVCAL_15	FAST/SLOW/MEDIUM	None
HSLVCAL_18	FAST/SLOW/MEDIUM	None

- GTP_OUTBUFT

Port descriptions are as follows:

Table 18 GTP_OUTBUFT port description

Port	Direction	Functional description
I	IN	Single-ended signal input
O	OUT	buffer output
T	IN	Enable signal, 1 is valid

The parameter description is as follows:

Table 19 GTP_OUTBUFT parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	See Table 20	"LVCMOS33"	Input IO standard
SLEW_RATE	string	"SLOW" ,"MEDIUM", "FAST"	"SLOW"	Slew rate
DRIVE_STRENGTH	string	"2", "4", "6", "8", "12", "16", "24"	"8"	Drive current strength

The list of valid values for the parameters is as follows:

Table 20 List of Valid Values of Parameters

GTP_OUTBUFT		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
LVTTL33	FAST/SLOW	"4", "8", "12", "16", "24"
PCI33	None	None
LVCMOS33	FAST/SLOW	"4", "8", "12", "16"
LVCMOS25	FAST/SLOW	"4", "8", "12", "16"
LVCMOS18	FAST/SLOW/MEDIUM	"2", "4", "6", "8", "12", "16", "24"
LVCMOS15	FAST/SLOW/MEDIUM	"2", "4", "6", "8", "12", "16"
LVCMOS12	FAST/SLOW/MEDIUM	"2", "4", "6", "8"
SSTL18_I	FAST/SLOW/MEDIUM	None
SSTL18_II	FAST/SLOW/MEDIUM	None
SSTL15_I	FAST/SLOW/MEDIUM	None
SSTL15_II	FAST/SLOW/MEDIUM	None
SSTL135_I	FAST/SLOW/MEDIUM	None
SSTL135_II	FAST/SLOW/MEDIUM	None
SSTL12	FAST/SLOW/MEDIUM	None
HSTL18_I	FAST/SLOW/MEDIUM	None
HSTL18_II	FAST/SLOW/MEDIUM	None
HSTL15_I	FAST/SLOW/MEDIUM	None
HSTL15_II	FAST/SLOW/MEDIUM	None
HSTL12_I	FAST/SLOW/MEDIUM	None
HSUL12	FAST/SLOW/MEDIUM	None
POD12	FAST/SLOW/MEDIUM	None
SSTL18_I_CAL	FAST/SLOW/MEDIUM	None
SSTL18_II_CAL	FAST/SLOW/MEDIUM	None
SSTL15_I_CAL	FAST/SLOW/MEDIUM	None
SSTL15_II_CAL	FAST/SLOW/MEDIUM	None
SSTL135_I_CAL	FAST/SLOW/MEDIUM	None
SSTL135_II_CAL	FAST/SLOW/MEDIUM	None
SSTL12_CAL	FAST/SLOW/MEDIUM	None
HSTL18_I_CAL	FAST/SLOW/MEDIUM	None
HSTL18_II_CAL	FAST/SLOW/MEDIUM	None
HSTL15_I_CAL	FAST/SLOW/MEDIUM	None
HSTL15_II_CAL	FAST/SLOW/MEDIUM	None
HSTL12_I_CAL	FAST/SLOW/MEDIUM	None
HSUL12_CAL	FAST/SLOW/MEDIUM	None
POD12_CAL	FAST/SLOW/MEDIUM	None
LVCAL_15	FAST/SLOW/MEDIUM	None
LVCAL_18	FAST/SLOW/MEDIUM	None
HSLVCAL_15	FAST/SLOW/MEDIUM	None

GTP_OUTBUFT		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
HSLVCAL_18	FAST/SLOW/MEDIUM	None

- GTP_IOBUF

Port descriptions are as follows:

Table 21 GTP_IOBUF port description

Port	Direction	Functional description
I	IN	Single-ended signal input
O	OUT	The output of the input buffer is sent to the chip
T	IN	Enable output buffer
IO	INOUT	Input and output signals (inout)

The parameter description is as follows:

Table 22 GTP_IOBUF parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	See Table 23	"LVCMOS33"	Input IO standard
TERM_DDR	string	"ON", "OFF"	"ON"	HSTL, SSTL standard input, the built-in terminal resistor is enabled or disabled
SLEW_RATE	string	"SLOW", "MEDIUM", "FAST"	"SLOW"	Slew rate
DRIVE_STRENGTH	string	"4", "6", "8", "12", "16", "24"	"8"	Drive current strength

The list of valid values for the parameters is as follows:

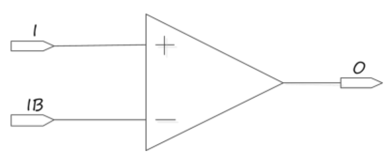
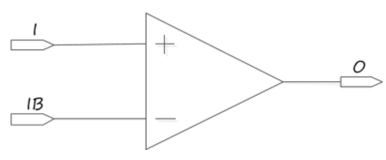
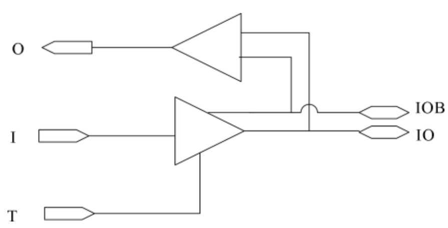
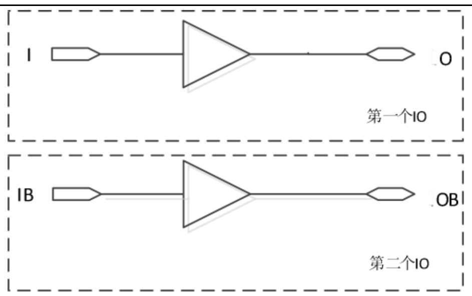
Table 23 List of valid values of parameters

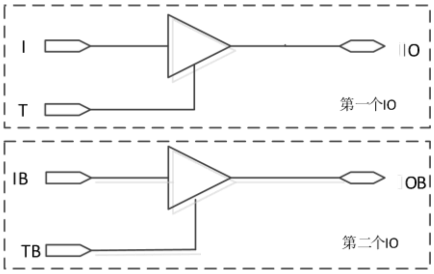
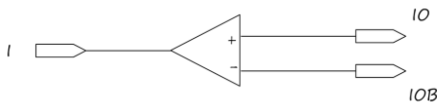
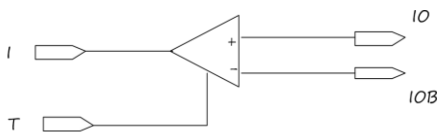
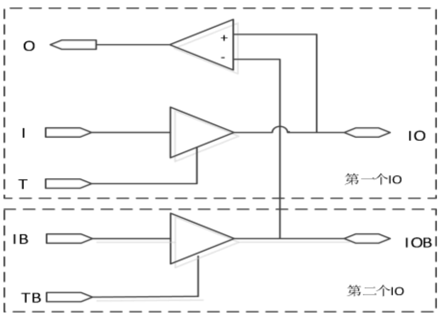
GTP_IOBUF			
IOSTANDARD	SLEW_RATE	TERM_DDR	DRIVE_STRENGTH
LVTTL33	FAST/SLOW	None	"4", "8", "12", "16", "24"
PCI33	None	None	None
LVCMOS33	FAST/SLOW	None	"4", "8", "12", "16"
LVCMOS25	FAST/SLOW	None	"4", "8", "12", "16"
LVCMOS18	FAST/SLOW/MEDIUM	None	"2", "4", "6", "8", "12", "16", "24"
LVCMOS15	FAST/SLOW/MEDIUM	None	"2", "4", "6", "8", "12", "16"
LVCMOS12	FAST/SLOW/MEDIUM	None	"2", "4", "6", "8"
SSTL18_I	FAST/SLOW/MEDIUM	OFF/ON	None
SSTL18_II	FAST/SLOW/MEDIUM	OFF/ON	None
SSTL15_I	FAST/SLOW/MEDIUM	OFF/ON	None
SSTL15_II	FAST/SLOW/MEDIUM	OFF/ON	None
SSTL135_I	FAST/SLOW/MEDIUM	OFF/ON	None
SSTL135_II	FAST/SLOW/MEDIUM	OFF/ON	None
SSTL12	FAST/SLOW/MEDIUM	OFF/ON	None
HSTL18_I	FAST/SLOW/MEDIUM	OFF/ON	None
HSTL18_II	FAST/SLOW/MEDIUM	OFF/ON	None
HSTL15_I	FAST/SLOW/MEDIUM	OFF/ON	None
HSTL15_II	FAST/SLOW/MEDIUM	OFF/ON	None
HSUL12_I	FAST/SLOW/MEDIUM	OFF/ON	None
HSUL12	FAST/SLOW/MEDIUM	OFF/ON	None

GTP_IOBUF			
IOSTANDARD	SLEW_RATE	TERM_DDR	DRIVE_STRENGTH
POD12	FAST/SLOW/MEDIUM	OFF/ON	None
SSTL18_I_CAL	FAST/SLOW/MEDIUM	ON	None
SSTL18_II_CAL	FAST/SLOW/MEDIUM	ON	None
SSTL15_I_CAL	FAST/SLOW/MEDIUM	ON	None
SSTL15_II_CAL	FAST/SLOW/MEDIUM	ON	None
SSTL135_I_CAL	FAST/SLOW/MEDIUM	ON	None
SSTL135_II_CAL	FAST/SLOW/MEDIUM	ON	None
SSTL12_CAL	FAST/SLOW/MEDIUM	ON	None
HSTL18_I_CAL	FAST/SLOW/MEDIUM	ON	None
HSTL18_II_CAL	FAST/SLOW/MEDIUM	ON	None
HSTL15_I_CAL	FAST/SLOW/MEDIUM	ON	None
HSTL15_II_CAL	FAST/SLOW/MEDIUM	ON	None
HSUL12_CAL	FAST/SLOW/MEDIUM	ON	None
POD12_CAL	FAST/SLOW/MEDIUM	ON	None
LVCAL_15	FAST/SLOW/MEDIUM	None	None
LVCAL_18	FAST/SLOW/MEDIUM	None	None
HSLVCAL_15	FAST/SLOW/MEDIUM	None	None
HSLVCAL_18	FAST/SLOW/MEDIUM	None	None

The table below lists the most commonly used GTPs for differential I/O.

Table 24 GTP for Differential I/O

GTP Name	Meaning	Schematic diagram
GTP_INBUFDS	Support differential input drive function, INBUFDS has 2 inputs I and IB, respectively representing the P-channel input pin and N-channel input pin of the differential pair	
GTP_INBUFGDS	Supports differential input for clock	
GTP_IOBUFDS	Support true differential input and output	
GTP_OUTBUFCO_E1	HP IO support class differential output drive function	

GTP Name	Meaning	Schematic diagram
GTP_OUTBUFTCO_E1	HP IO supports class differential output drive function and tri-state output	
GTP_OUTBUFDS	Support true differential output function. Supported IO input standards are: "LVDS", "MINI-LVDS" and "TMDS"	
GTP_OUTBUFTDS	Support true differential output function. Supported IO input standards are: "LVDS", "MINI-LVDS", "TMDS"	
GTP_IOBUFCO_E1	HP IO supports single-ended input, differential-like output drive function	

➢ GTP_INBUFDS

Port descriptions are as follows:

Table 25 GTP_INBUFDS port description

Port	Direction	Functional description
I	IN	Non-inverting differential input
IB	IN	Inverting differential input
O	OUT	Differential output, sent to the chip

The parameter description is as follows:

Table 26 GTP_INBUFDS parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	See Table 27	LVDS	Input IO standard
TERM_DIFF	string	See Table 27	ON	For differential input, the built-in terminal resistor is enabled or disabled

The list of valid values for the parameters is as follows:

Table 27 List of valid values for parameters

GTP_INBUFDS	
IOSTANDARD	**TERM_DIFF**
LVDS_18	OFF/ON
LVDS	OFF/ON
MINI-LVDS	OFF/ON
SUB-LVDS	OFF/ON
TMDS	OFF/ON
PPDS	OFF/ON
RSDS	OFF/ON
GTP_INBUFDS	
IOSTANDARD	**TERM_DIFF**
LVDS_18	OFF/ON
LVDS	OFF/ON
MINI-LVDS	OFF/ON
SUB-LVDS	OFF/ON
TMDS	OFF/ON
PPDS	OFF/ON
RSDS	OFF/ON

- GTP_INBUFGDS

Port descriptions are as follows:

Table 28 GTP_INBUFGDS port description

Port	Direction	Functional description
I	IN	Non-inverting differential input
IB	IN	Inverting differential input
O	OUT	Differential output, sent to the chip

The parameter description is as follows:

Table 29 GTP_INBUFGDS parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	See Table 30	LVDS	Input IO standard
TERM_DIFF	string	See Table 30	ON	For differential input, the built-in terminating resistor is turned on or off

The list of valid values for the parameters is as follows:

Table 30 List of Valid Values for Parameters

GTP_INBUFGDS	
IOSTANDARD	**TERM_DIFF**
LVDS_18	OFF/ON
LVDS	OFF/ON
MINI-LVDS	OFF/ON
SUB-LVDS	OFF/ON
TMDS	OFF/ON
PPDS	OFF/ON
RSDS	OFF/ON

- GTP_IOBUFDS

Port descriptions are as follows:

Table 31 GTP_IOBUFDS port description

Port	Direction	Functional description
I	IN	Single-ended signal input
O	OUT	Input buffer output, sent to the chip
T	IN	Enable signal
IO	INOUT	IO PADs
IOB	INOUT	IO's PAD, opposite to IO's value

The parameter description is as follows:

Table 32 GTP_IOBUFDS parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	"LVDS", "MINI-LVDS", "PPDS", "RSDS", "SUB-LVDS", "TMDS", "LVDS_18"	LVDS	Input IO standard
TERM_DIFF	string	"ON", "OFF"	ON	For standard input such as LVDS, the built-in differential termination resistor is turned on or off

- GTP_OUTBUFCO_E1

Port descriptions are as follows:

Table 33 GTP_OUTBUFCO_E1 port description

Port	Direction	Functional description
I	IN	The first IO single-ended signal input
IB	IN	The second IO single-ended signal input, its value is the inverse of I
O	INOUT	PAD of the first IO
OB	INOUT	The PAD of the second IO, its value is the inverse of IO

The parameter description is as follows:

Table 34 GTP_OUTBUFCO_E1 parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	"SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "SSTL135D_I", "SSTL135D_II", "SSTL12D", "HSTL15D_I", "HSTL15D_II", "HSTL18D_I", "HSTL18D_II", "HSTL12D_I", "HSUL12D", "POD12D", "SSTL18D_I_CAL", "SSTL18D_II_CAL", "SSTL15D_I_CAL", "SSTL15D_II_CAL", "SSTL135D_I_CAL", "SSTL135D_II_CAL", "SSTL12D_CAL", "HSTL15D_I_CAL", "HSTL15D_II_CAL", "HSTL18D_I_CAL", "HSTL18D_II_CAL", "HSTL12D_I_CAL", "HSUL12D_CAL", "POD12D_CAL"	POD12D	Input IO standard

- GTP_OUTBUFTCO_E1

Port descriptions are as follows:

Table 35 GTP_OUTBUFTCO_E1 port description

Port	Direction	Functional description
I	IN	Single-ended signal input
IB	IN	Single-ended signal input, its value is the inverse of I
T	IN	Enable output buffer
TB	IN	Enable output buffer
O	OUT	PAD of the first IO
OB	OUT	The PAD of the second IO, its value is the opposite of O

The parameter description is as follows:

Table 36 GTP_OUTBUFTCO_E1 parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	"SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "SSTL135D_I", "SSTL135D_II", "SSTL12D", "HSTL15D_I", "HSTL15D_II", "HSTL18D_I", "HSTL18D_II", "HSTL12D_I", "HSUL12D", "POD12D", "SSTL18D_I_CAL", "SSTL18D_II_CAL", "SSTL15D_I_CAL", "SSTL15D_II_CAL", "SSTL135D_I_CAL", "SSTL135D_II_CAL", "SSTL12D_CAL", "HSTL15D_I_CAL", "HSTL15D_II_CAL", "HSTL18D_I_CAL", "HSTL18D_II_CAL", "HSTL12D_I_CAL", "HSUL12D_CAL", "POD12D_CAL"	POD12D	Input IO standard

- GTP_OUTBUFDS

Port descriptions are as follows:

Table 37 GTP_OUTBUFDS port description

Port	Direction	Functional description
I	IN	Single-ended signal input
O	OUT	Differential P-side output
OB	OUT	Differential N-terminal output

The parameter description is as follows:

Table 38 GTP_OUTBUFDS parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	"LVDS", "MINI-LVDS", "SUB-LVDS", "TMDS", "RSDS", "PPDS", "LVDS_18"	LVDS	Input IO standard

- GTP_OUTBUFTDS

Port descriptions are as follows:

Table 39 GTP_OUTBUFTDS port description

Port	Direction	Functional description
I	IN	Single-ended signal input
O	OUT	PAD of the first IO
OB	OUT	The PAD of the second IO, its value is the inverse of the first IO
T	IN	enable signal

The parameter description is as follows:

Table 40 GTP_OUTBUFTDS parameter description

Name	Type	Valid values	Defaults	Functional description
IOSTANDARD	string	"LVDS", "MINI-LVDS", "SUB-LVDS", "TMDS", "RSDS", "PPDS", "LVDS_18"	LVDS	Input IO standard

- GTP_IOBUFCO_E1

Port descriptions are as follows:

Table 41 GTP_IOBUFCO_E1 port description

Port	Direction	Functional description
I	IN	The first IO single-ended signal input
IB	IN	The second IO single-ended signal input
O	OUT	PAD of the first IO
OB	OUT	The PAD of the second IO, its value is the inverse of IO

The parameter description is as follows:

Table 42 GTP_IOBUFCO_E1 parameter description

Name	Settings	Defaults	Functional description
IOSTANDARD	See Table 43, Table 44	DEFAULT = POD12D	Input IO standard
TERM_DDR	"ON", "OFF"	"ON"	HSTL, SSTL standard input, the built-in terminal resistor is enabled or disabled

Table 43 GTP_IOBUFCO_E1 parameter valid value list (Titan2 HPIO)

GTP_IOBUFCO_E1 (Titan2 HPIO)	
IOSTANDARD	TERM_DDR
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
SSTL135D_I	OFF/ON
SSTL135D_II	OFF/ON

GTP_IOBUFCO_E1 (Titan2 HPIO)	
IOSTANDARD	TERM_DDR
SSTL12D	OFF/ON
HSTL12D_I	OFF/ON
HSTL15D_I	OFF/ON
HSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSUL12D	OFF/ON
POD12D	OFF/ON
SSTL18D_I_CAL	ON
SSTL18D_II_CAL	ON
SSTL15D_I_CAL	ON
SSTL15D_II_CAL	ON
SSTL135D_I_CAL	ON
SSTL135D_II_CAL	ON
SSTL12D_CAL	ON
HSTL12D_I_CAL	ON
HSTL15D_I_CAL	ON
HSTL15D_II_CAL	ON
HSTL18D_I_CAL	ON
HSTL18D_II_CAL	ON
HSUL12D_CAL	ON
POD12D_CAL	ON

Table 44 GTP_IOBUFCO_E1 parameter valid value list (Titan2 HRIO)

GTP_IOBUFCO_E1 (Titan2 HRIO)	
IOSTANDARD	TERM_DDR
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON

GTP_IOBUFCO_E1 (Titan2 HRIO)	
IOSTANDARD	TERM_DDR
SSTL135D_I	OFF/ON
SSTL135D_II	OFF/ON
HSTL15D_I	OFF/ON
HSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSUL12D	OFF/ON

16. IO SSN

SSN (Simultaneous Switching Noise) is synchronous switching noise, which is mainly introduced by the power distribution network and mutual inductance crosstalk, which will produce a certain voltage drop at high level and a certain ground bounce at low level. I/O standard tolerance, it may be considered as an effective signal inversion, resulting in a functional error of the system. The I/O resources of the FPGA chip are distributed in each bank, and each bank has its own independent power distribution network, the impact of SSN noise in different banks is different. In addition, the I/O Standard and the number of I/Os in the bank will also affect the SSN noise in the bank.

The Pango Design Suite software includes Pango SSN Analyzer (referred to as PNA) and Pango SSN Estimator (referred to as PNE). The PNA analysis tool combines the I/O pin information assigned by the user in the IO Planner and the voltage characteristics of each bank to predict Analyze the SSN noise interference of each I/O port in the bank, and evaluate the size of its margin, so that users can understand the potential SSN noise risk in the design. For details, see "Pango SSN Analyzer User Manual V1.0". PNE main application In the early design stage of PCB, users can adjust the I/O allocation of desige according to the estimated SSN results. PNE software can estimate the worst-case noise of high and low levels of remote victim pins when multiple aggressor I/Os are switched at the same time, see "Pango SSN Estimator User Manual V1.0" for details.

(3) IO LOGIC

This section mainly describes the IOL part of Titan2 series products.

The IOL is between the IOB and the internal logic of the FPGA, and performs some processing on the data before entering or outputting from the FPGA. The IOL includes input and output delay chain units, input logic (ILOGIC) and output logic (OLOGIC). The structure is shown in the following block diagram.

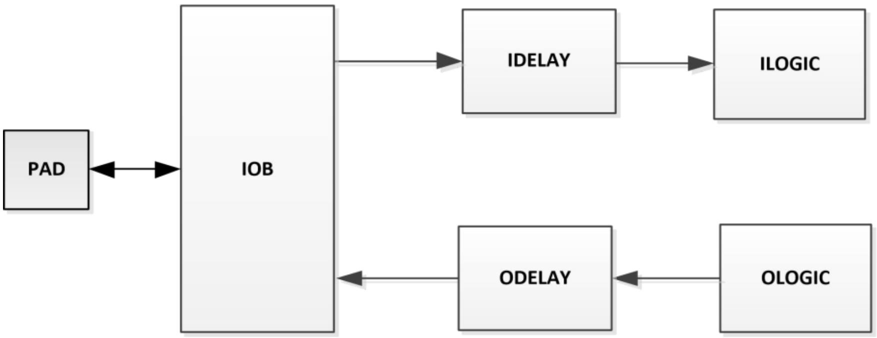


Figure 9 IOL block diagram

1. Input and output delay chain unit

Each I/O PAD contains an IO DELAY unit, which can be used for input or output delay. For HR BANK, the maximum input delay is 2.47ns, and the maximum output delay is 635ps. For HP BANK, the maximum input delay is 2.226ns, and the maximum output delay is the delay is 571.5ps, which can provide static configuration or dynamic adjustment DELAY mode. IO DELAY is often used to adjust the sampling window or adjust the output timing.

The PDS software provides special primitives for the use of input and output delay chains. For HR BANK, the input delay chain primitive is GTP_IODELAY_E2 or GTP_ZEROHOLDDELAY, and the output delay chain primitive is GTP_IODELAY_E2. For HP BANK input and output delay the chain primitive is GTP_IODELAY_E2. GTP_IODELAY_E2 is used for the delay of all bank clocks and data, and GTP_ZEROHOLDDELAY is only used for the delay of HR BANK data. The following is the structure diagram of the two.

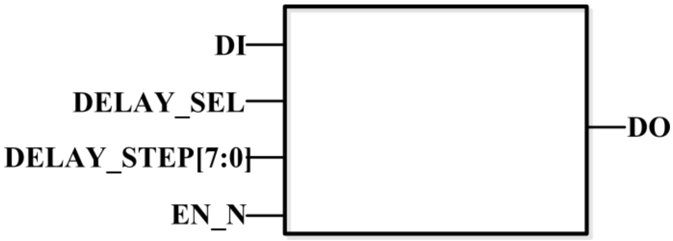


Figure 10 GTP_IODELAY_E2 structure diagram



Figure 11 GTP_ZEROHOLDDELAY structure diagram

GTP_IODELAY_E2 is instantiated in Verilog as follows:

```
GTP_IODELAY_E2 #(
.DELAY_STEP_VALUE('b00000000),
.DELAY_STEP_SEL("PARAMETER"),
.TDELAY_EN("FALSE")
) <InstanceName> (
.DELAY_STEP(DELAY_STEP),
.DO(DO),
.DELAY_SEL(DELAY_SEL),
.DI(DI),
.EN_N(EN_N)
);
```

The parameters and signals of the GTP_IODELAY_E2 prototype module are described as follows:

Table 45 GTP_IODELAY_E2 port description

Port Signal	Input/Output	Width	Description
DI	Input	1 bit	Input data
DELAY_SEL	Input	1 bit	Step mode selection, when DELAY_SEL is 0, HR IO input, output delay is delayed by 5ps per STEP, HP IO input, output delay is delayed by 4.5ps per STEP; when DELAY_SEL is 1, HR IO input delay is delayed by each STEP 10ps, HR IO output delay is 5ps per STEP, HP IO input delay is 10ps per STEP, HP IO output delay is 4.5ps per STEP.
DELAY_STEP	Input	8 bit	Delay step size, the actual maximum effective value for input delay is 8’d247, and the maximum effective value for output delay is 8’d127, the input type must be gray code
EN_N	Input	1bit	Active low signal
DO	Output	1 bit	Data output

Note: STEP is a typical value

Table 46 GTP_IODELAY_E2 parameter description

Name	Type	Settings	Defaults	Functional description
DELAY_STEP_SEL	String	"PARAMETER" "PORT"	"PARAMETER"	"PARAMETER": select static configuration; "PORT": dynamic configuration
DELAY_STEP_VALUE	Constant	8’h00~8’hF7	8’h00	idelay delay control code static configuration (Gray code)
TDLY	String	"FALSE" "TRUE"	"FALSE"	"TRUE": Map Titan2 HPIO Tdelay function

GTP_ZEROHOLDDELAY is instantiated in Verilog as follows:

```
GTP_ZEROHOLDDELAY #(
.ZHOLD_SET("NODELAY")
) <InstanceName> (
.DO(DO),
.DI(DI)
);
```

Table 47 GTP_ZEROHOLDDELAY port description

Port Signal	Input/Output	Width	Description
DI	Input	1 bit	Data input
DO	Output	1 bit	Data output

Table 48 GTP_ZEROHOLDDELAY parameter description

Name	Type	Valid values	Defaults	Functional description
ZHOLD_SET	String	"NODELAY", "100ps", "200ps", "300ps", "400ps", "500ps", "600ps", "700ps", "800ps", "900ps", "1000ps", "1100ps", "1200ps", "1300ps", "1400ps", "1500ps"	"NODELAY"	zeroholddelay delay value

2. Input Logic

The input logic of the IOL is used to process the received high-speed data and realize the conversion of high-speed serial data into parallel data. In order to realize the serial-to-parallel conversion function in the IOL, for HR BANK and HP BANK, PDS provides the GTP_ISERDES_E2 primitive, and GTP_ISERDES_E2 is used as input Data processing in the direction, support directly input and output, iLatch, IDFF, networking SDR/DDR, Oversample, Low-Speed Memory DDR, High-Speed Memory DDR, and support SDR1TO2, SDR1TO3, SDR1TO4, SDR1TO5, SD R1TO6, SDR1TO7, SDR1TO8, DDR1TO2_SAME_PIPELINED, DDR1TO2_SAME_EDGE, DDR1TO2_OPPOSITE_EDGE, DDR1TO4, DDR1TO6, DDR1TO8, DDR1TO10, DDR1TO14, HMDDR1TO4, HMDDR1TO8, LMDDR1TO4, LMDDR1TO8 and OVERSAMPLE mode rate conversion. The structure diagram is as follows:

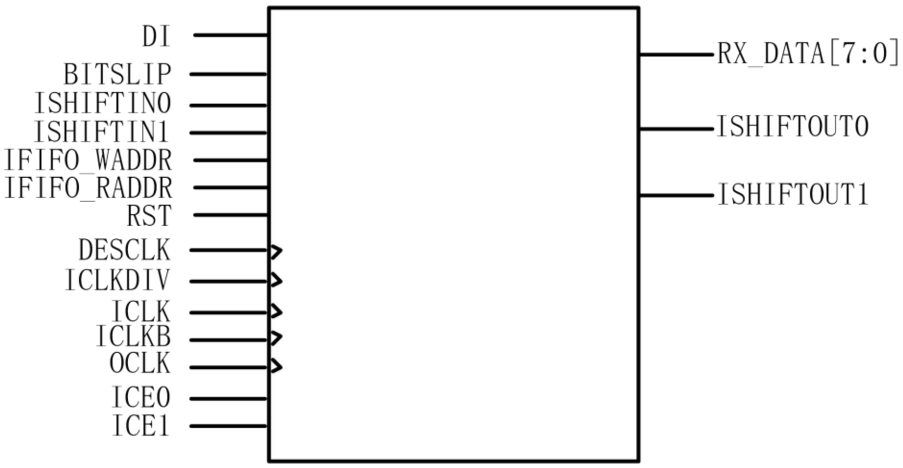


Figure 12 GTP_ISERDES_E2 structure diagram

GTP_ISERDES_E2 is instantiated in Verilog as follows:

```
GTP_ISERDES_E2 #(
.ISERDES_MODE("SDR1TO4"),
.GRS_EN("TRUE"),
.CASCADE_MODE("MASTER"),
.BITSLIP_EN("FALSE"),
.NUM_ICE(0),
.GRS_TYPE_Q0("RESET"),
.GRS_TYPE_Q1("RESET"),
.GRS_TYPE_Q2("RESET"),
.GRS_TYPE_Q3("RESET"),
.LRS_TYPE_Q0("ASYNC_RESET"),
.LRS_TYPE_Q1("ASYNC_RESET"),
.LRS_TYPE_Q2("ASYNC_RESET"),
.LRS_TYPE_Q3("ASYNC_RESET"),
.HPIO("FALSE")
) <InstanceName> (
.DO(DO),
.IFIFO_RADDR(IFIFO_RADDR),
.IFIFO_WADDR(IFIFO_WADDR),
.ISHIFTOUT0(ISHIFTOUT0),
.ISHIFTOUT1(ISHIFTOUT1),
.BITSLIP(BITSLIP),
.DESCLK(DESCLK),
.DI(DI),
.ICE0(ICE0),
.ICE1(ICE1),
.ICLK(ICLK),
.ICLKB(ICLKB),
.ICLKDIV(ICLKDIV),
.ISHIFTIN0(ISHIFTIN0),
.ISHIFTIN1(ISHIFTIN1),
.OCLK(OCLK),
.RST(RST)
);
```

GTP_ISERDES_E2 is usually used together with GTP_INBUF, GTP_INBUFG, GTP_INBUFDS and GTP_INBUFGDS.

Table 49 GTP_ISERDES_E2 parameter description

Name	Type	Settings	Defaults	Functional description
HPIO	String	"TRUE" "FALSE"	"FALSE"	"TRUE" maps to HPIO, "FALSE" maps to HRIO
ISERDES_MODE	String	"SDR1TO2"	SDR1TO4	"SDR1TO2": networking SDR 1:2 deserialization mode

Name	Type	Settings	Defaults	Functional description
		"SDR1TO3"		"SDR1TO3": networking SDR 1:3 deserialization mode
		"SDR1TO4"		"SDR1TO4": networking SDR 1:4 deserialization mode
		"SDR1TO5"		"SDR1TO5": networking SDR 1:5 deserialization mode
		"SDR1TO6"		"SDR1TO6": networking SDR 1:6 deserialization mode
		"SDR1TO7"		"SDR1TO7": networking SDR 1:7 deserialization mode
		"SDR1TO8"		"SDR1TO8": networking SDR 1:8 deserialization mode
		"ILATCH"		"ILATCH" Latch input mode
		"IDFF"		"IDFF" register input mode
		"DDR1TO2_SAME_PIPELINED"		"DDR1TO2_same_piplelined": networking DDR 1:2 same pipelined deserialization mode
		"DDR1TO2_SAME_EDGE"		"DDR1TO2_SAME_EDGE": networking DDR 1:2 SAME_EDGE deserialization mode
		"DDR1TO2_OPPOSITE_EDGE"		"DDR1TO2_OPPOSITE_EDGE": networking DDR 1:2 OPPOSITE_EDGE deserialization mode
		"DDR1TO4"		"DDR1TO4": networking DDR 1:4 deserialization mode
		"DDR1TO6"		"DDR1TO6": networking DDR 1:6 deserialization mode
		"DDR1TO8"		"DDR1TO8": networking DDR 1:8 deserialization mode
		"DDR1TO10 "		"DDR1TO10": networking DDR 1:10 deserialization mode
		"DDR1TO14"		"DDR1TO14": networking DDR 1:14 deserialization mode

Name	Type	Settings	Defaults	Functional description
		"HMDDR1TO4" "HMDDR1TO8" "LMDDR1TO4" "LMDDR1TO8" "OVERSAMPLE		"HMDDR1TO4": High-Speed Memory DDR 1:4 deserialization mode "HMDDR1TO8": High-Speed Memory DDR 1:8 deserialization mode "LMDDR1TO4": Low-Speed Memory DDR 1:4 deserialization mode "LMDDR1TO8": Low-Speed Memory DDR 1:8 deserialization mode "OVERSAMPLE" deserialization mode
CASCADE_MODE	String	"MASTER" "SLAVE"	"MASTER"	Deserialized cascaded master mode
BITSLIP_EN	String	"FALSE" "TRUE"	"FALSE"	bitslip enable
GRS_EN	String	"TRUE" "FALSE"	"TRUE"	Global reset/set enable
NUM_ICE	Constance	1’b0 1’b1	1’b0	ice number selection
GRS_TYPE_Q0	String	"RESET" "SET"	"RESET"	DFF0 global asynchronous reset/set result in ILOGIC gear;
GRS_TYPE_Q1	String	"RESET" "SET"	"RESET"	DFF1 global asynchronous reset/set result in ILOGIC gear;
GRS_TYPE_Q2	String	"RESET" "SET"	"RESET"	DFF2 global asynchronous reset/set result in ILOGIC gear;
GRS_TYPE_Q3	String	"RESET" "SET"	"RESET"	DFF3 global asynchronous reset/set result in ILOGIC gear;
LRS_TYPE_Q0	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF0 local asynchronous/synchronous/reset/set result in ILOGIC gear
LRS_TYPE_Q1	String	"ASYNC_RESET" "ASYNC_SET"	"ASYNC_RESET"	DFF1 local asynchronous/ synchronous/ reset/set result in ILOGIC gear

Name	Type	Settings	Defaults	Functional description
		"SYNC_RESET" "SYNC_SET"		
LRS_TYPE_Q2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF2 local async/sync/reset/set result in ILOGIC gear
LRS_TYPE_Q3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF3 local async/sync/reset/set result in ILOGIC gear

Note: For the use of HMDDR and LMDDR modes in the table, when the rate is equal to or greater than 500Mbps, HMDDR mode must be used; when the rate is less than 500Mbps, both HMDDR mode and LMDDR mode can be used.

Table 50 GTP_ISERDES_E2 port description

Port Signal	Input/Output	Description
DI	Input	Data input
BITSLIP	Input	Data input
ISHIFTIN0	Input	Cascade input signal
ISHIFTIN1	Input	Cascade input signal
IFIFO_WADDR	Input	FIFO write address DQS falling edge trigger (Gray code)
IFIFO_RADDR	Input	FIFO read address (Gray code)
RST	Input	ILOGIC's local reset signal (need to be valid for at least two ICLKDIV clock cycles), active high
DESCLK	Input	ILOGIC deserialization high-speed clock (DESCLK and ICLKDIV are synchronous clocks)
ICLKDIV	Input	ILOGIC low speed clock
ICLK	Input	ILOGIC Level 1 High Speed Clock
ICLKB	Input	ILOGIC first-level high-speed clock reverse input (only as an emulation port, software does not map)
OCLK	Input	OLOGIC output stage high speed clock
ICE0	Input	Clock enable signal for ILOGIC
ICE1	Input	Clock enable signal for ILOGIC
DO	Output	Output signal after deserialization
ISHIFTOUT0	Output	Cascade output signal

Port Signal	Input/Output	Description
ISHIFTOUT1	Output	Cascaded output signal

Direct Input

The following describes the input logic configuration as direct input mode, which is divided into two modes: register input and latch input.

IDFF

When the Input logic is configured as IDFF mode, its function diagram can be simplified as the following diagram.



Figure 13 IDFF functional diagram

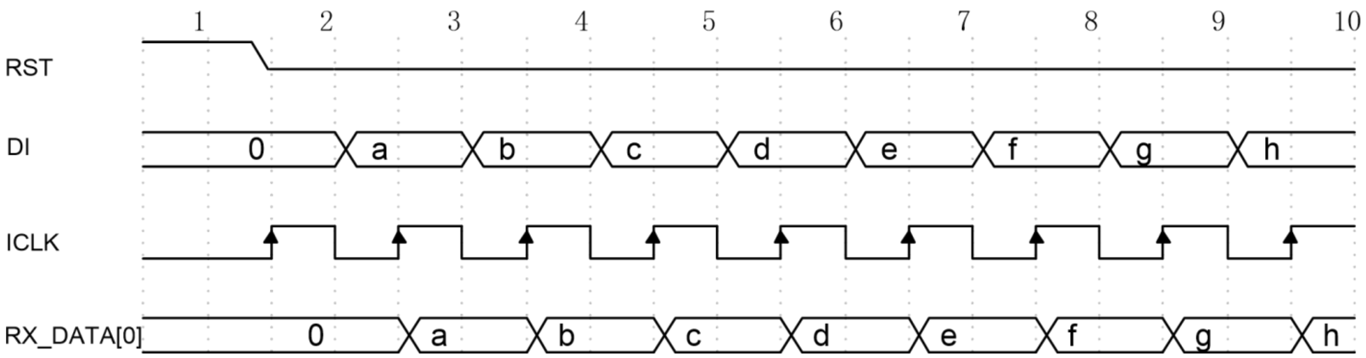


Figure 14 IDFF Timing Diagram

ILATCH

When the Input logic is configured as ILATCH mode, its function diagram can be simplified to the following diagram.



Figure 15 ILATCH Function Diagram

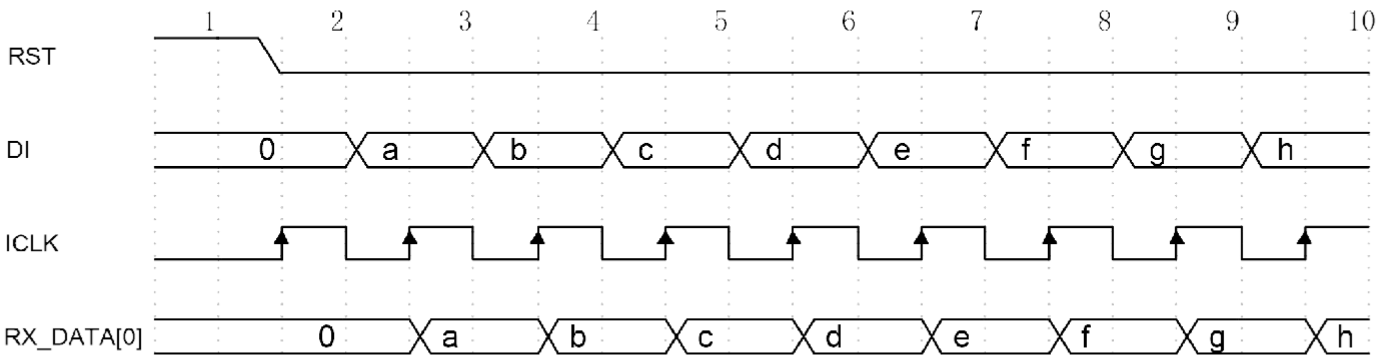


Figure 16 ILATCH Timing Diagram

IDDR

GTP_IDDR_E1 is a data deserializer, its structural block diagram is shown below, it supports OPPOSITE_EDGE, SAME_EDGE, SAME_PIPELINED modes.

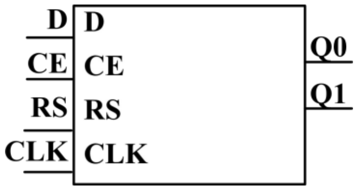


Figure 17 GTP_IDDR_E1 Structure Diagram

The Verilog instantiation of GTP_IDDR_E1 is as follows:

```
GTP_IDDR_E1 #(
.GRS_EN("TRUE"),
.IDDR_MODE("OPPOSITE_EDGE"),
.RS_TYPE("ASYNC_RESET")
) <InstanceName> (
.Q0(Q0),
.Q1(Q1),
.CE(CE),
.CLK(CLK),
.D(D),
.RS(RS)
);
```

Table 51 GTP_IDDR_E1 port description

Port Signal	Input/Output	Width	Description
D	Input	1	Data Input
CE	Input	1	Clock Enable
RS	Input	1	Set/Reset
CLK	Input	1	System Clock
Q0	Output	1	Deserialized output
Q1	Output	1	Deserialized output

Table 52 GTP_ IDDR_E1 parameter list description

Name	Type	Settings	Defaults	Functional description
IDDR_MODE	string	"SAME_PIPELINED" "SAME_EDGE" "OPPOSITE_EDGE"	"OPPOSITE_EDGE"	"SAME_PIPLELINED": DDR 1:2 same pipelined deserialization mode "SAME_EDGE": DDR 1:2 SAME_EDGE deserialization mode "OPPOSITE_EDGE": DDR 1:2 OPPOSITE_EDGE deserialization mode
RS_TYPE	string	"SYNC_SET" "ASYNC_SET" "SYNC_RESET" "ASYNC_RESET"	"ASYNC_RESET"	Reset/Set Mode Selection: Synchronous Set, Asynchronous Set, Synchronous Reset, Asynchronous Reset
GRS_EN	string	"FALSE" "TRUE"	"TRUE"	Global reset enable

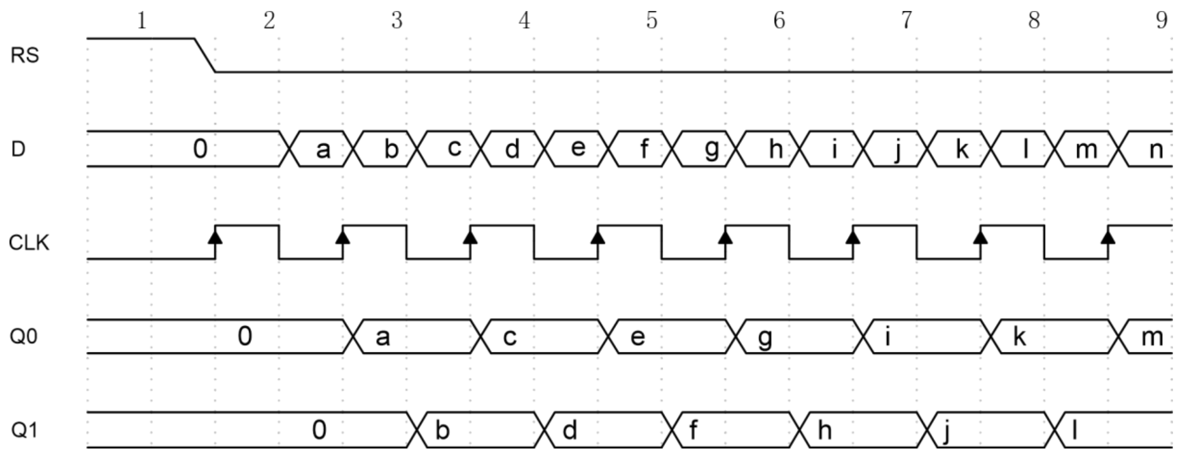


Figure 18 GTP_IDDR_E1 OPPOSITE_EDGE Mode Timing Diagram

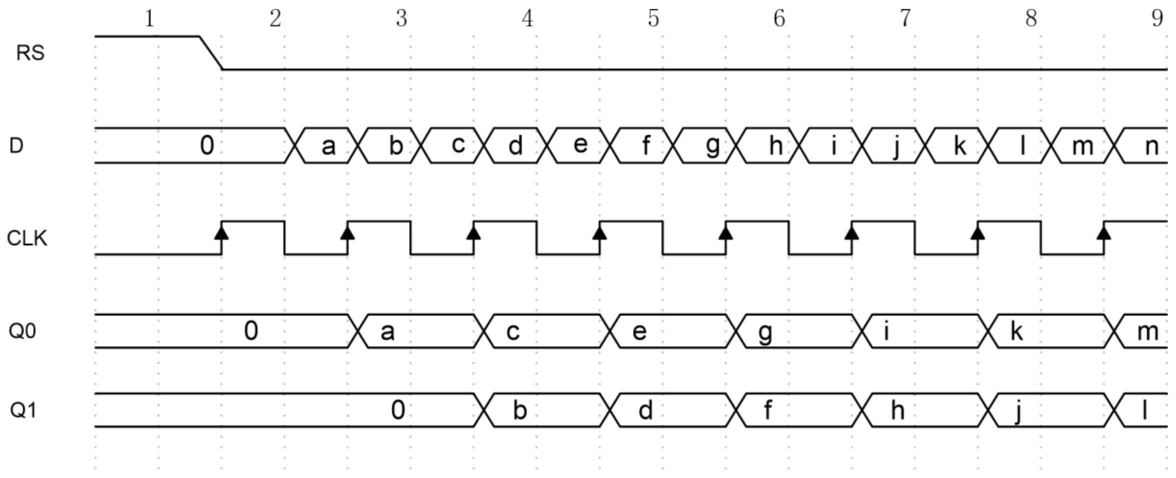


Figure 19 GTP_IDDR_E1 SAME_EDGE Mode Timing Diagram

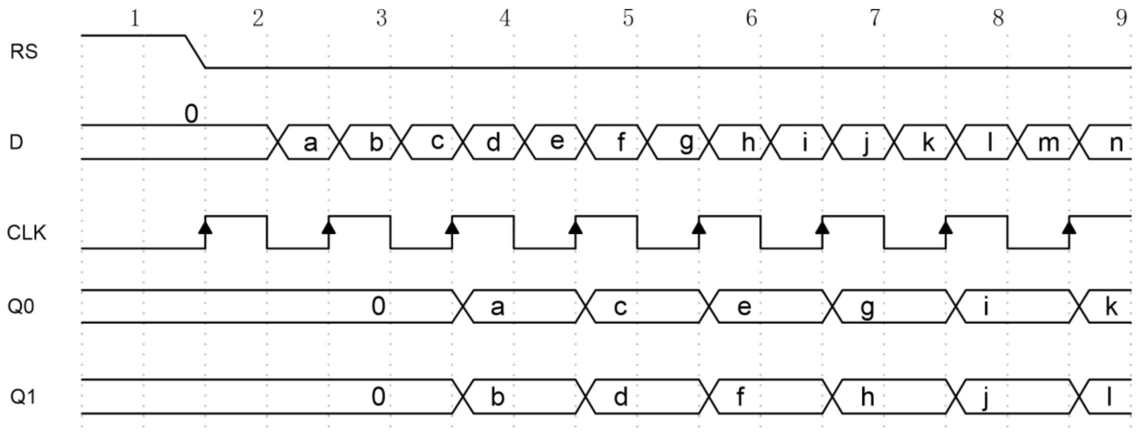


Figure 20 GTP_IDDR_E1 SAME_PIPELINED Mode Timing Diagram

ISERDES

The following describes the different working modes of Input logic configured as ISERDES.

SDR1TO2

When the Input logic is configured as SDR1TO2 mode, its function diagram can be simplified to the following diagram.

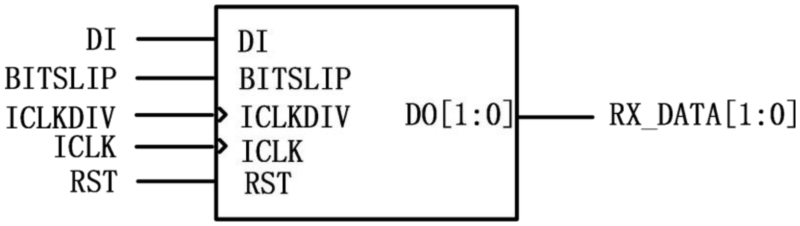


Figure 21 SDR1TO2 Function Diagram

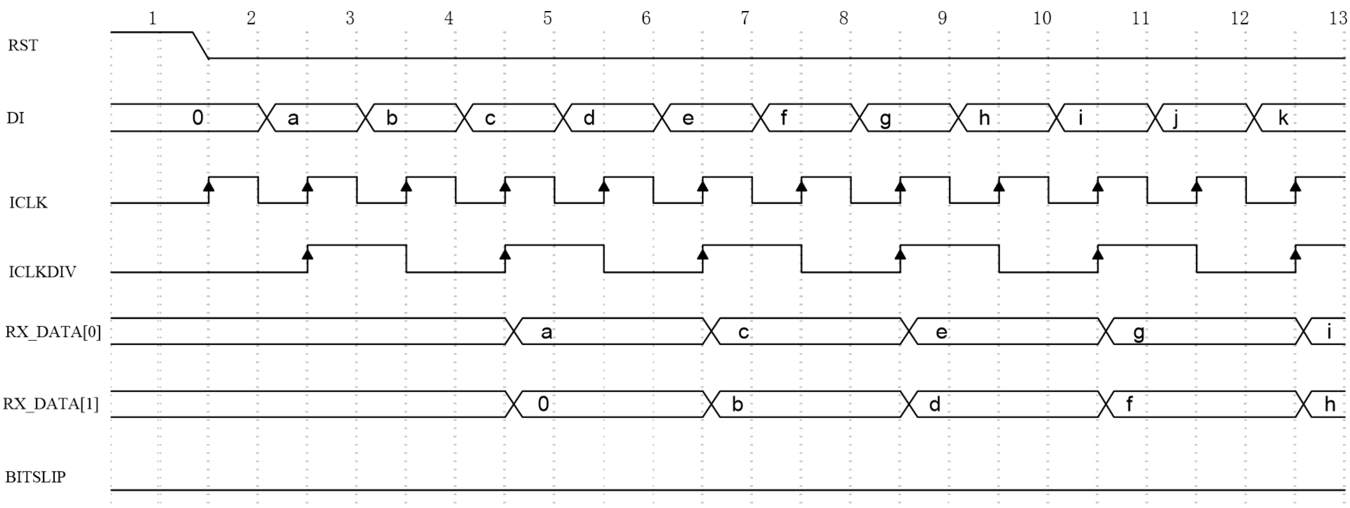


Figure 22 SDR1TO2 Timing Diagram

SDR1TO3

When the Input logic is configured as SDR1TO3 mode, its function diagram can be simplified to the following diagram.

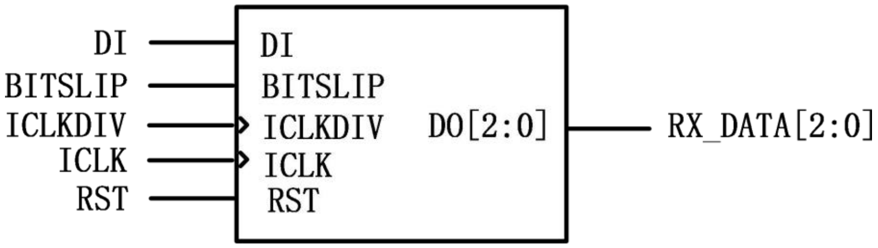


Figure 23 SDR1TO3 Function Diagram

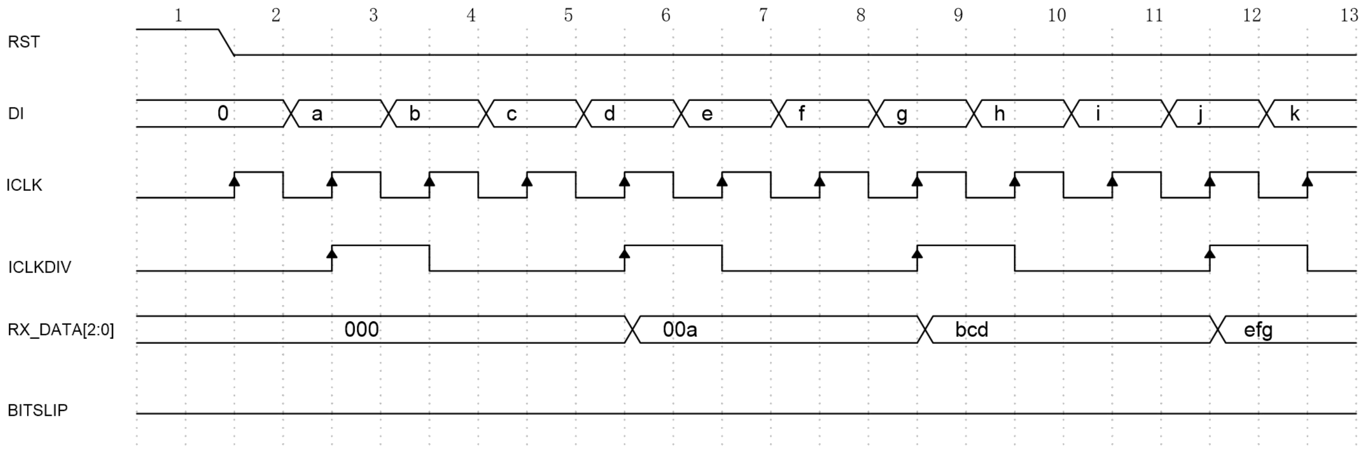


Figure 24 SDR1TO3 Timing Diagram

SDR1TO4

When the Input logic is configured as SDR1TO4 mode, its function diagram can be simplified to the following diagram.

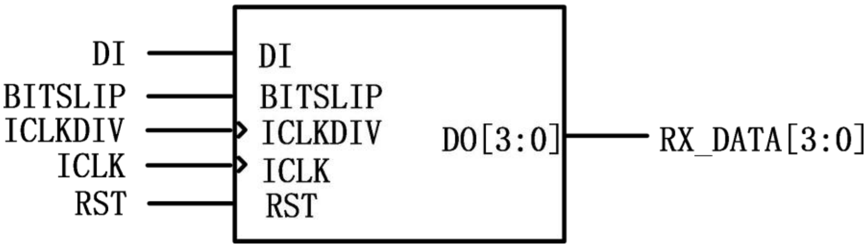


Figure 25 SDR1TO4 Function Diagram

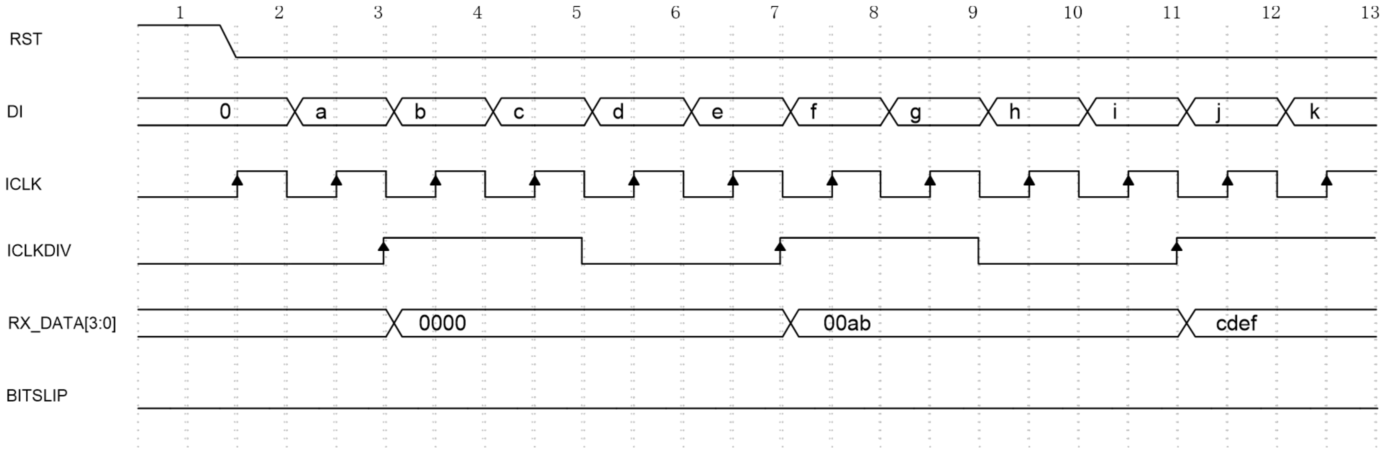


Figure 26 SDR1TO4 Timing Diagram

SDR1TO5

When the Input logic is configured as SDR1TO5 mode, its function diagram can be simplified as the following diagram.

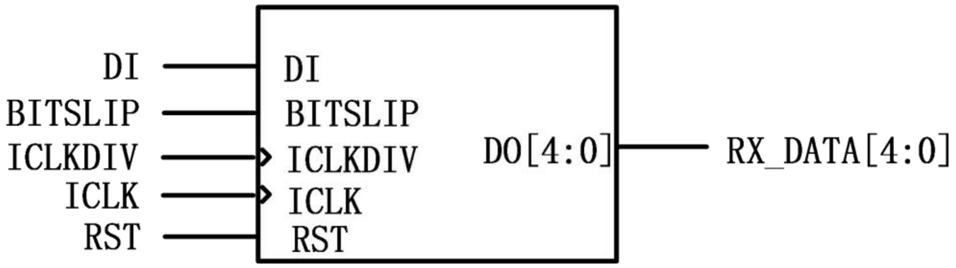


Figure 27 SDR1TO5 Function Diagram

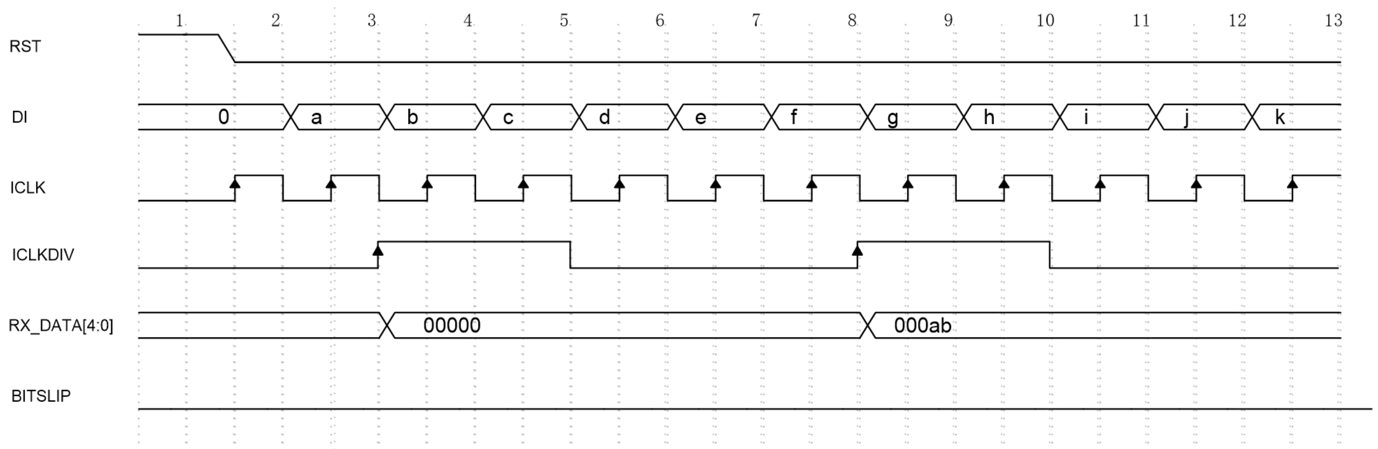


Figure 28 SDR1TO5 Timing Diagram

SDR1TO6

When the Input logic is configured as SDR1TO6 mode, its function diagram can be simplified as the following diagram.

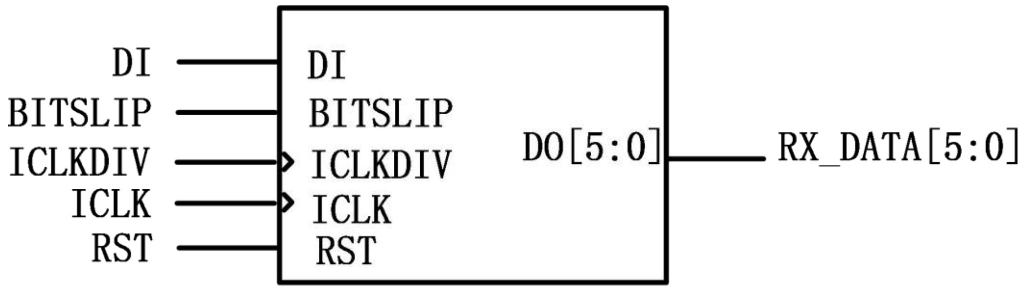


Figure 29 SDR1TO6 Function Diagram

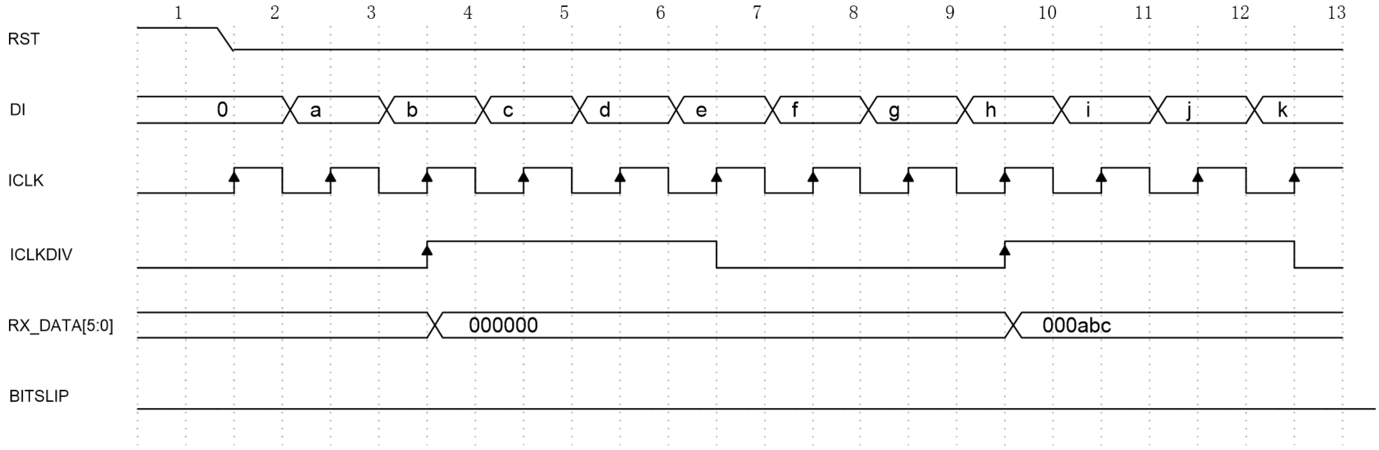


Figure 30 SDR1TO6 Timing Diagram

SDR1TO7

When the Input logic is configured as SDR1TO7 mode, its function diagram can be simplified to the following diagram.

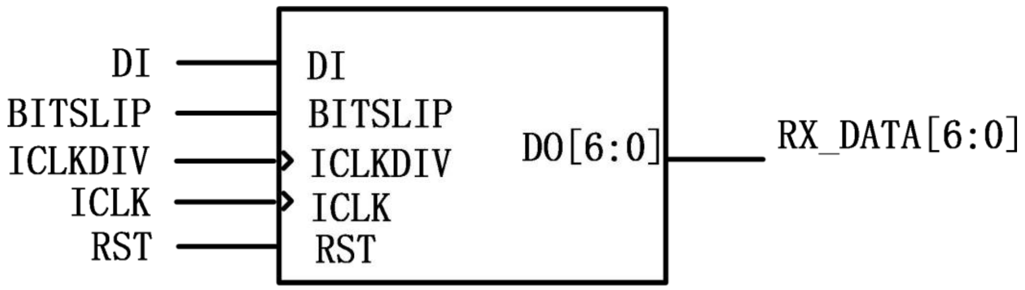


Figure 31 SDR1TO7 Function Diagram

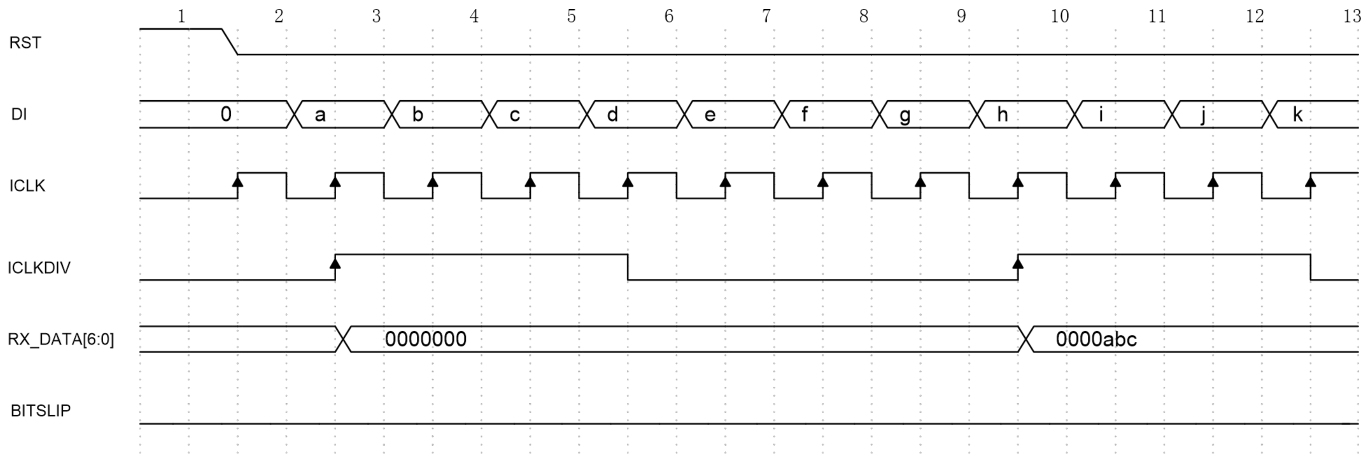


Figure 32 SDR1TO7 Timing Diagram

SDR1TO8

When the Input logic is configured as SDR1TO8 mode, its function diagram can be simplified to the following diagram.

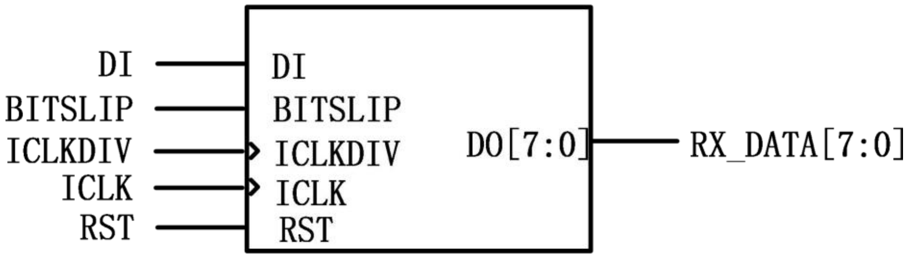


Figure 33 SDR1TO8 Function Diagram

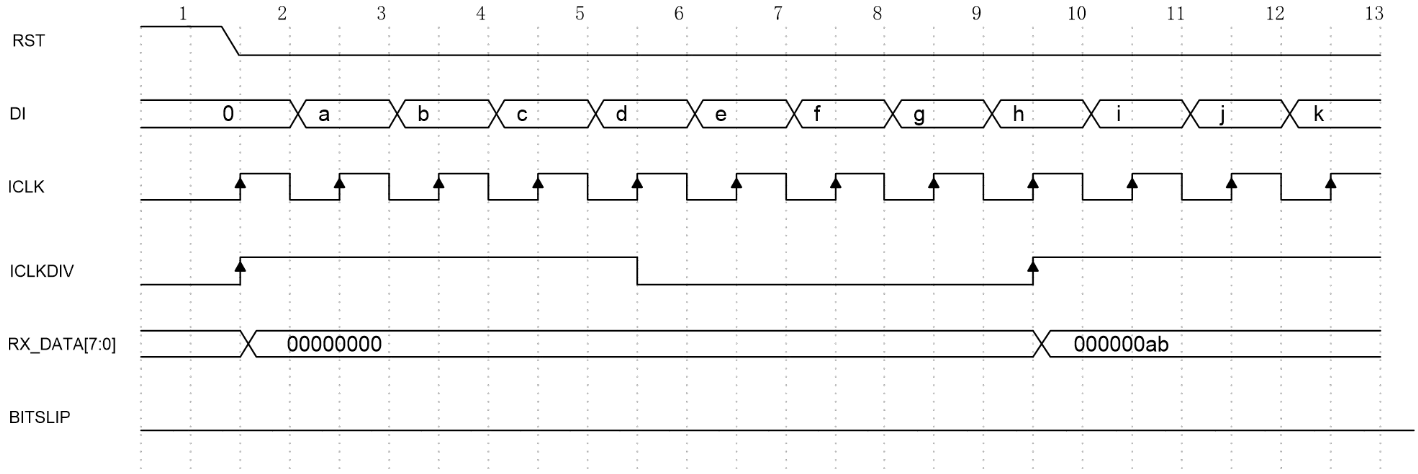


Figure 34 SDR1TO8 Timing Diagram

DDR1TO2_ OPPOSITE_EDGE

When the Input logic is configured as DDR1TO2_OPPOSITE_EDGE mode, its function diagram can be simplified as the following diagram.

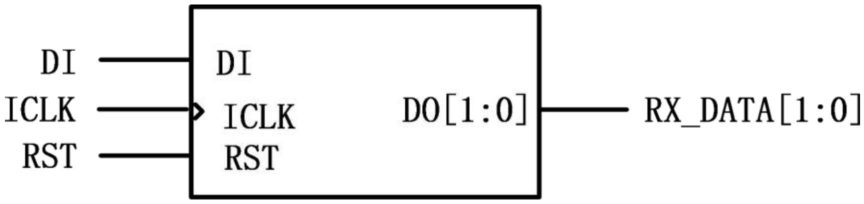


Figure 35 DDR1TO2_OPPOSITE_EDGE Function Diagram

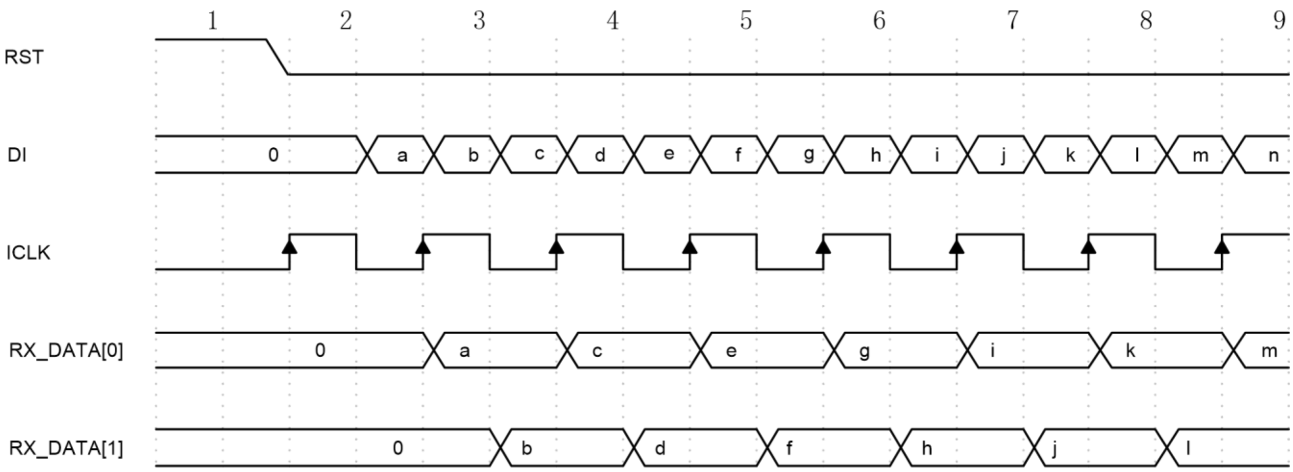


Figure 36 DDR1TO2_OPPOSITE_EDGE Timing Diagram

DDR1TO2_SAME_EDGE

When the Input logic is configured as DDR1TO2_SAME_EDGE mode, its function diagram can be simplified as the following diagram.

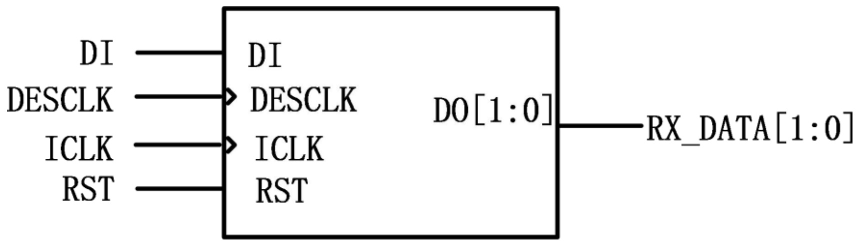


Figure 37 DDR1TO2_SAME_EDGE Function Diagram

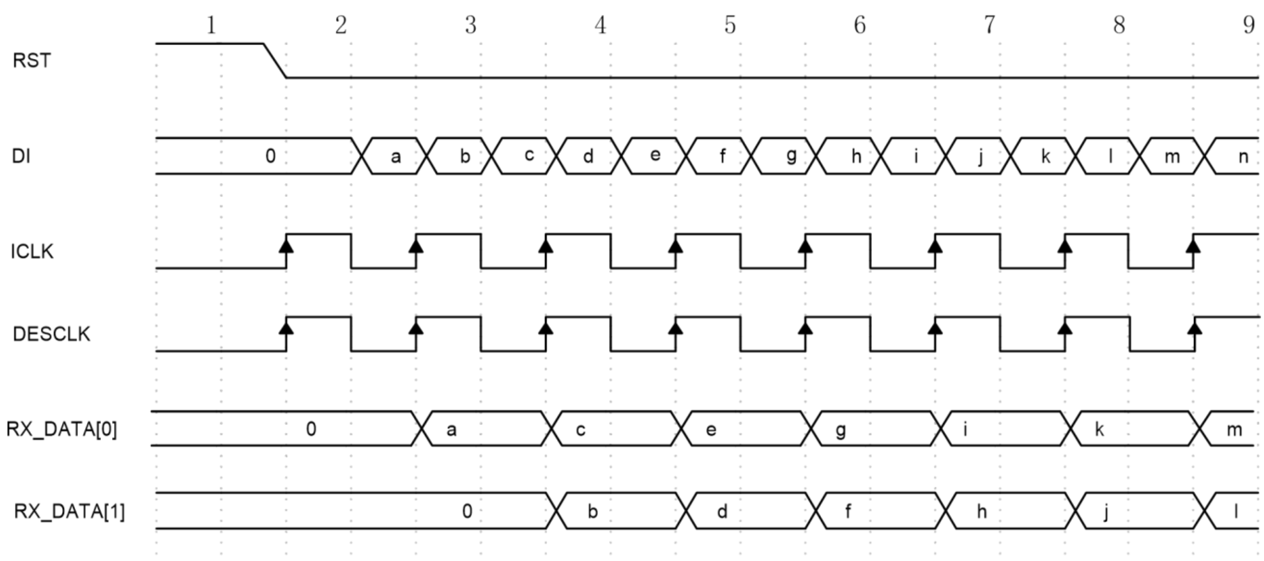


Figure 38 DDR1TO2_SAME_EDGE Timing Diagram

DDR1TO2_SAME_PIPELINED

When the Input logic is configured as DDR1TO2_SAME_PIPELINED mode, its function diagram can be simplified as the following diagram.

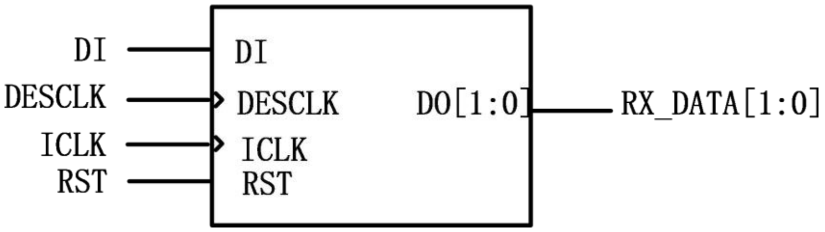


Figure 39 DDR1TO2_SAMEPIPELINE Function Diagram

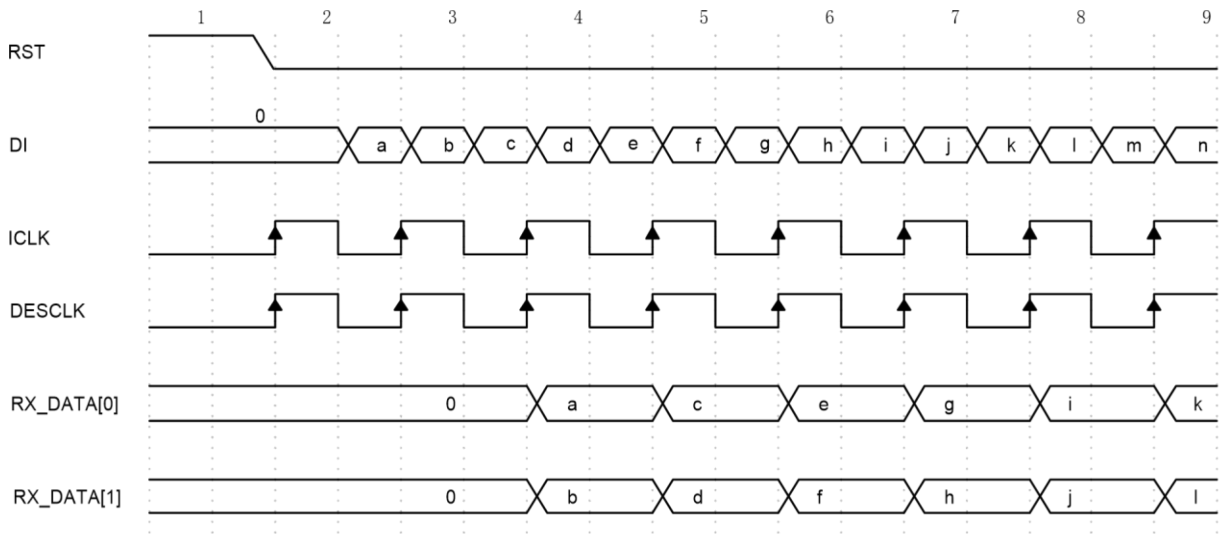


Figure 40 DDR1TO2_SAMEPIPELINE Timing Diagram

DDR1TO4

When the Input logic is configured as DDR1TO4 mode, its function diagram can be simplified as the following diagram.

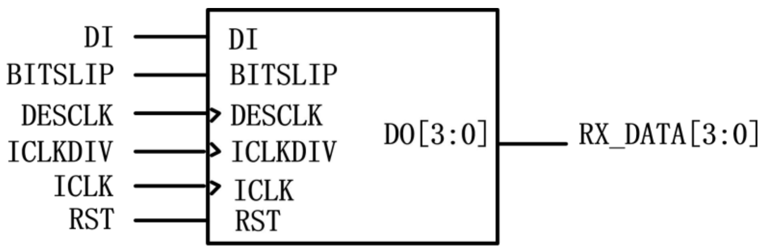


Figure 41 DDR1TO4 Function Diagram

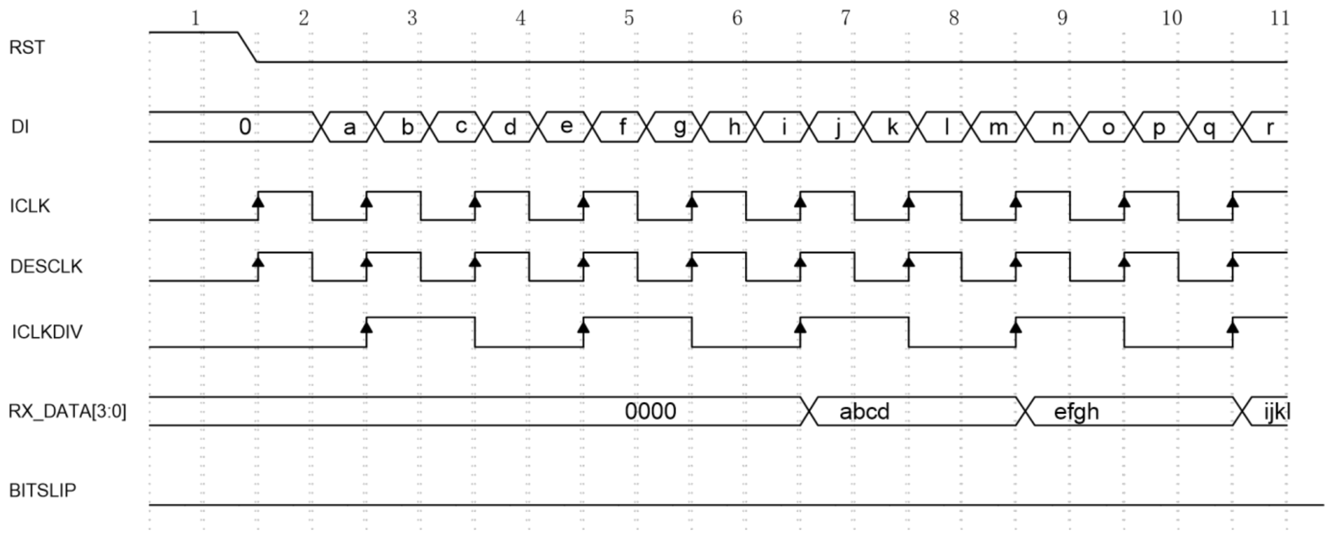


Figure 42 DDR1TO4 Timing Diagram

DDR1TO6

When the Input logic is configured as DDR1TO6 mode, its function diagram can be simplified as the following diagram.

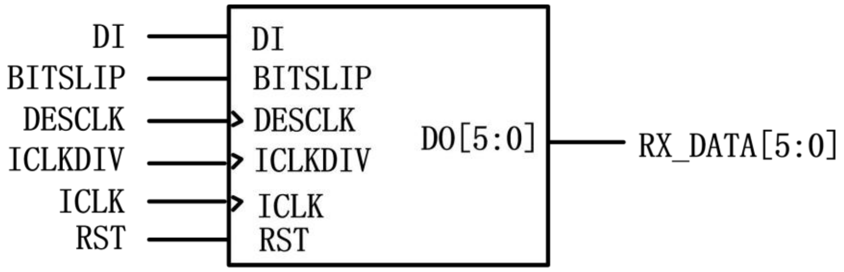


Figure 43 DDR1TO6 Function Diagram

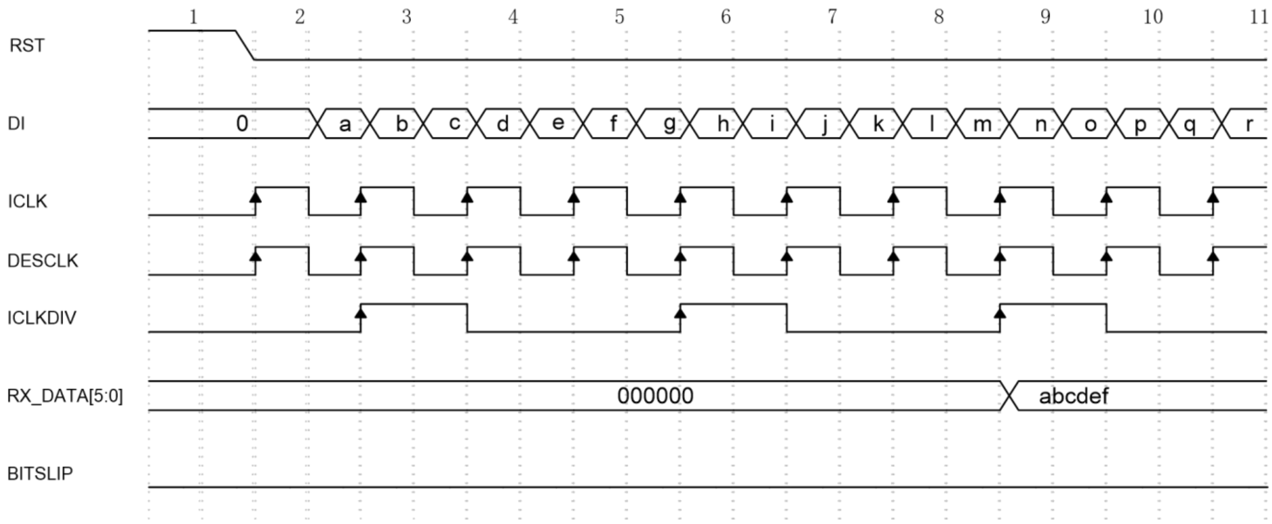


Figure 44 DDR1TO6 Timing Diagram

DDR1TO8

When the Input logic is configured as DDR1TO8 mode, its function diagram can be simplified as the following diagram.

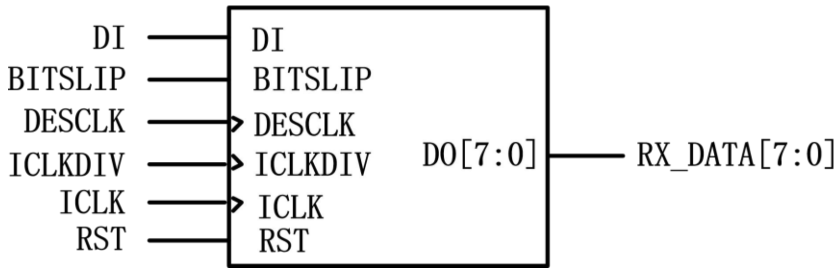


Figure 45 DDR1TO8 Function Diagram

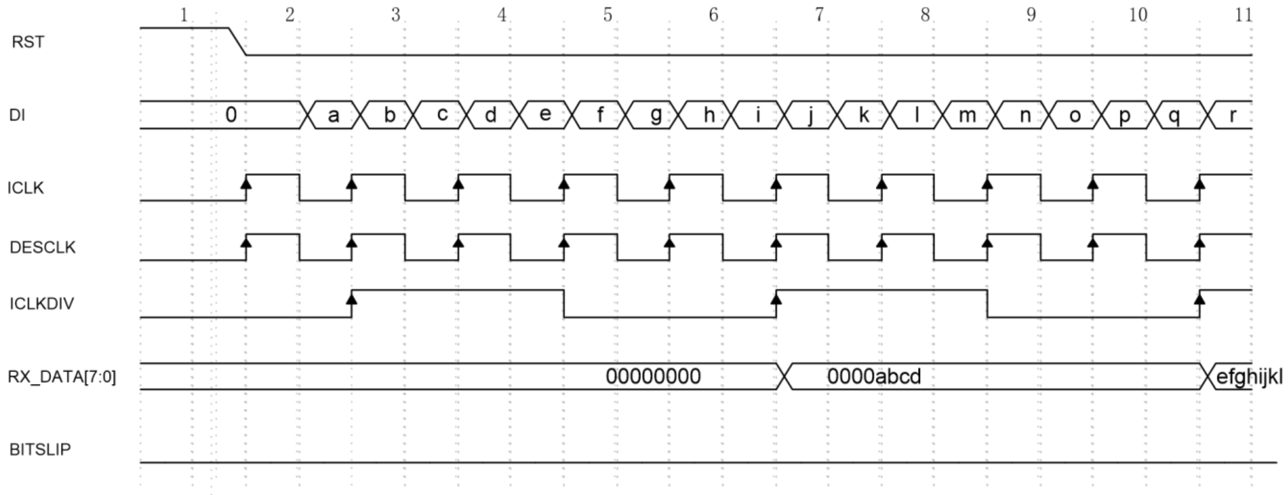


Figure 46 DDR1TO8 Timing Diagram

DDR1TO10

When the Input logic is configured as DDR1TO10 mode, two GTPs need to be instantiated, GTP_ISERDES_INST0 parameter CASCADE_MODE is set to "MASTER", GTP_ISERDES_INST1 parameter CASCADE_MODE is set to "SLAVE", its function diagram can be simplified as the following figure.

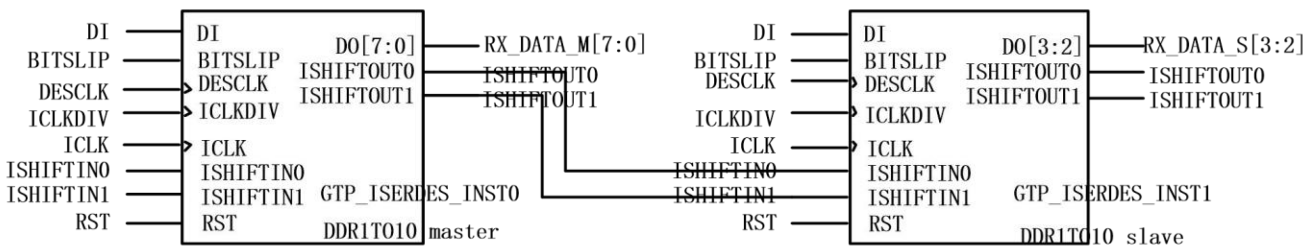


Figure 47 DDR1TO10 Function Diagram

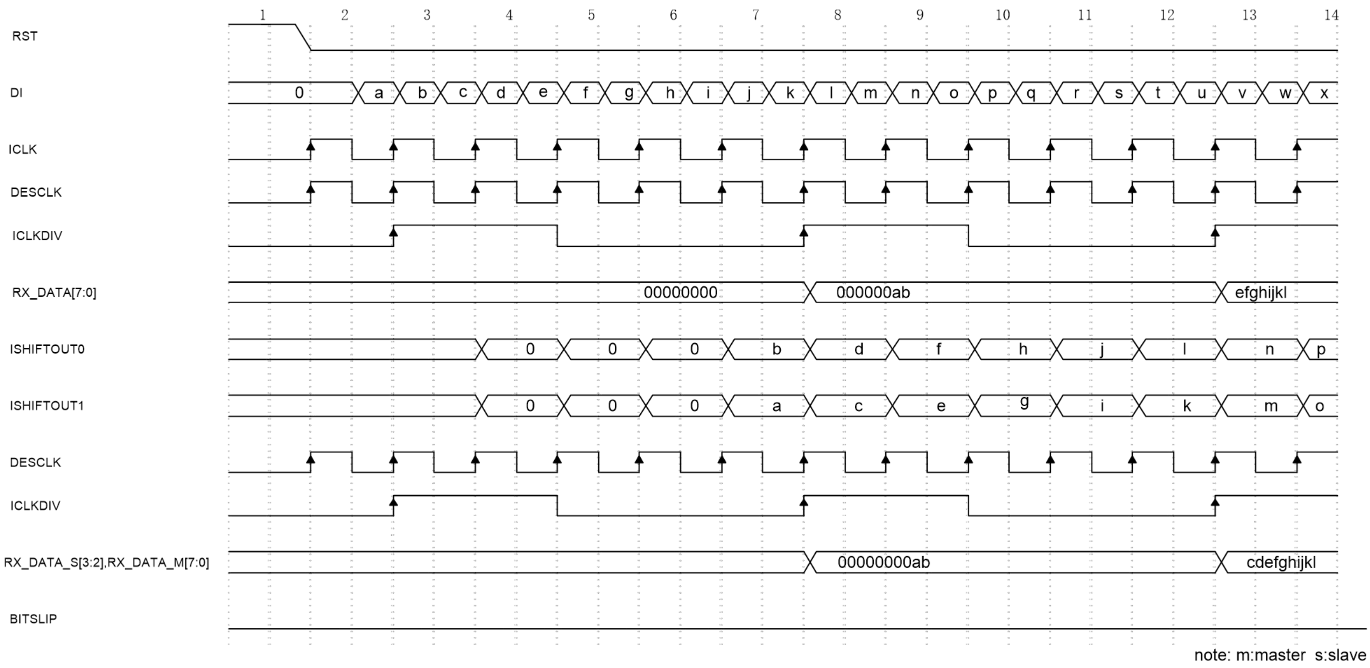


Figure 48 DDR1TO10 Timing Diagram

DDR1TO14

When the Input logic is configured as DDR1TO14 mode, two GTPs need to be instantiated, GTP_ISERDES_INST0 parameter CASCADE_MODE is set to "MASTER", GTP_ISERDES_INST1 parameter CASCADE_MODE is set to "SLAVE", and its function diagram can be simplified as the following figure.

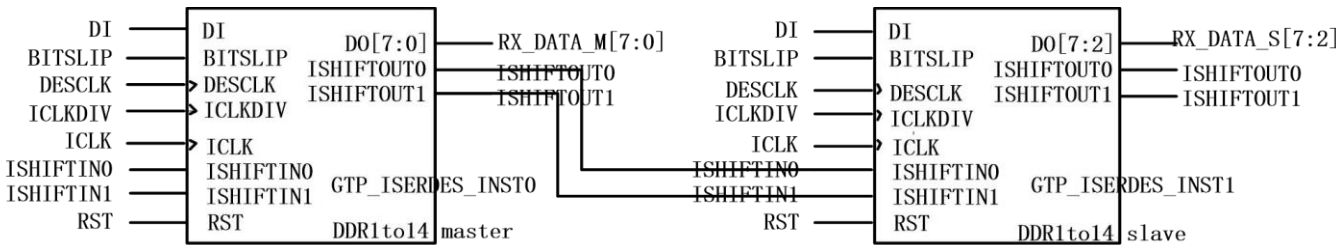


Figure 49 DDR1TO14 Function Diagram

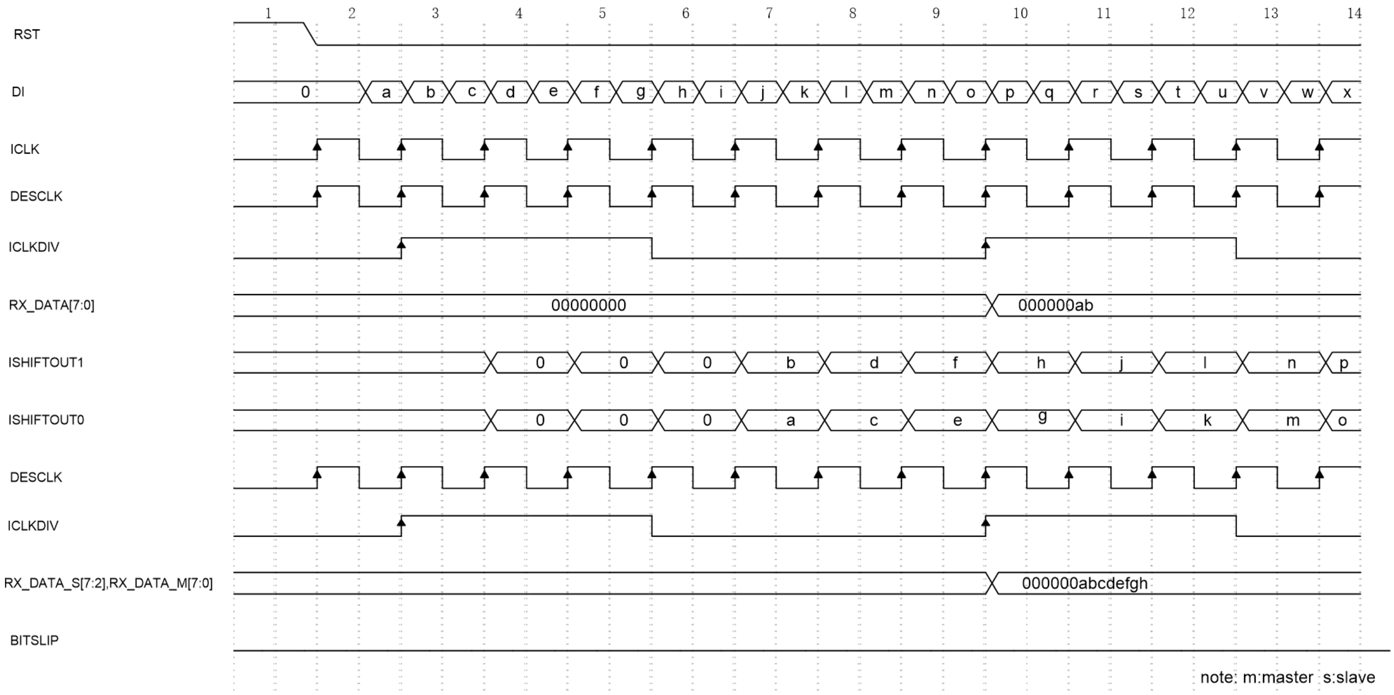


Figure 50 DDR1TO14 Timing Diagram

HMDDR1TO4

When the Input logic is configured as HMDDR1TO4 mode, its function diagram can be simplified as the following diagram.

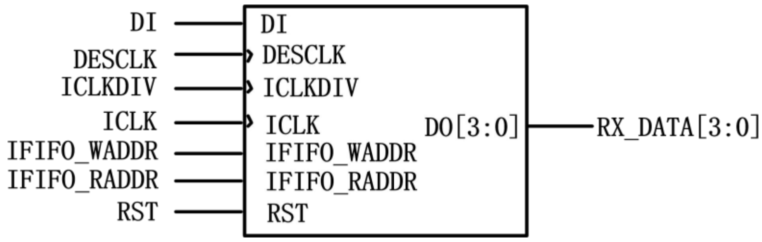


Figure 51 HMDDR1TO4 Function Diagram

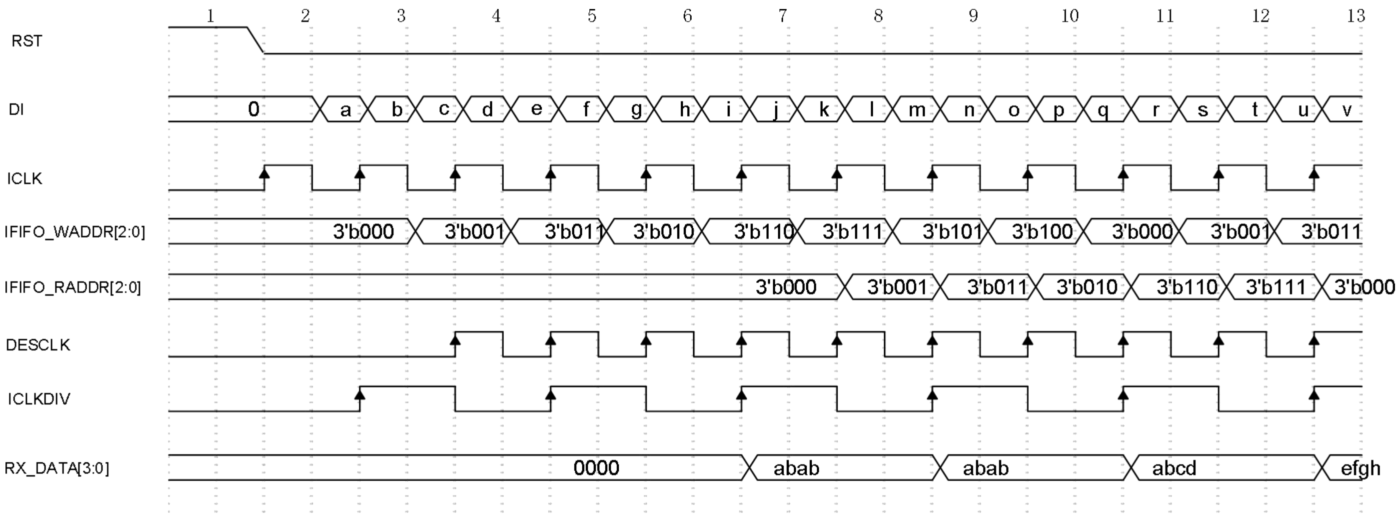


Figure 52 HMDDR1TO4 Timing Diagram

HMDDR1TO8

When the Input logic is configured as HMDDR1TO8 mode, its function diagram can be simplified to the following diagram.

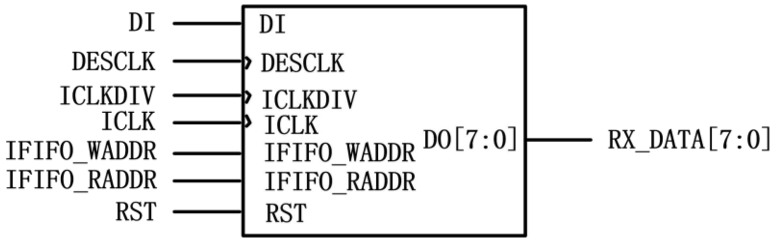


Figure 53 HMDDR1TO8 Function Diagram

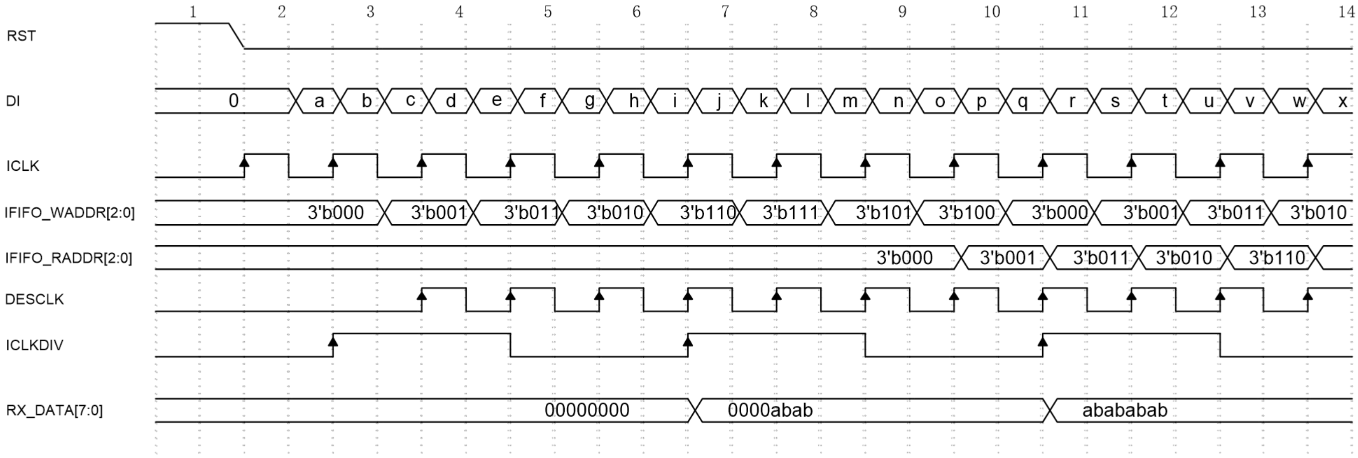


Figure 54 HMDDR1TO8 Timing Diagram

LMDDR1TO4

When the Input logic is configured as LMDDR1TO4 mode, its function diagram can be simplified as the following diagram.

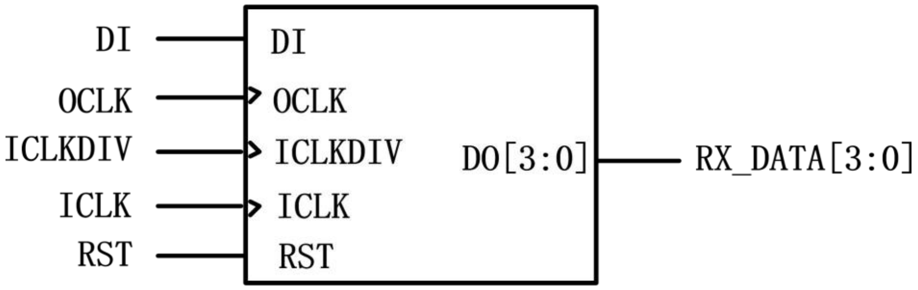


Figure 55 LMDDR1TO4 Function Diagram

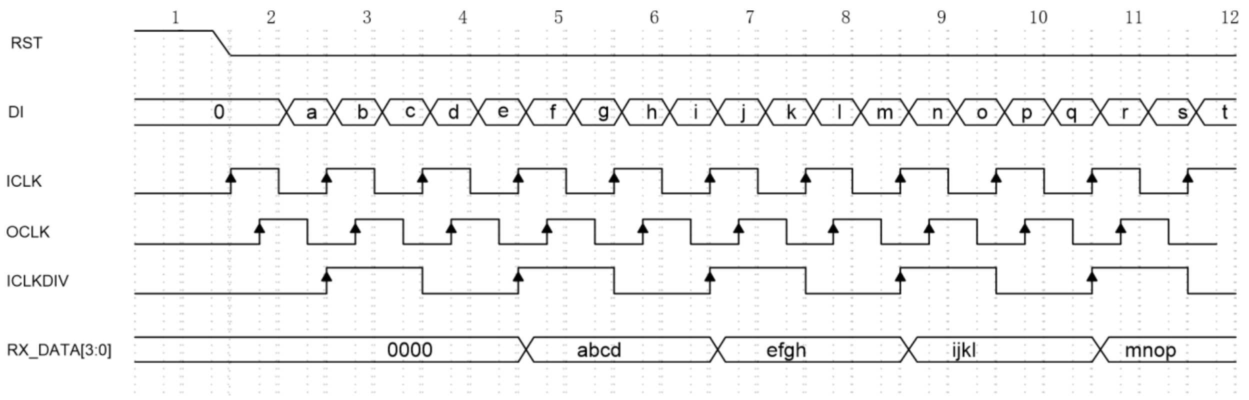


Figure 56 LMDDR1TO4 Timing Diagram

LMDDR1TO8

When the Input logic is configured as LMDDR1TO4 mode, its function diagram can be simplified as the following diagram.

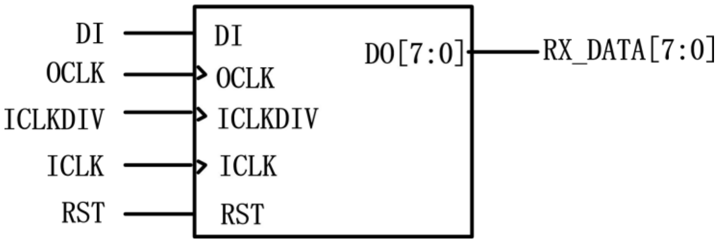


Figure 57 LMDDR1TO8 Function Diagram

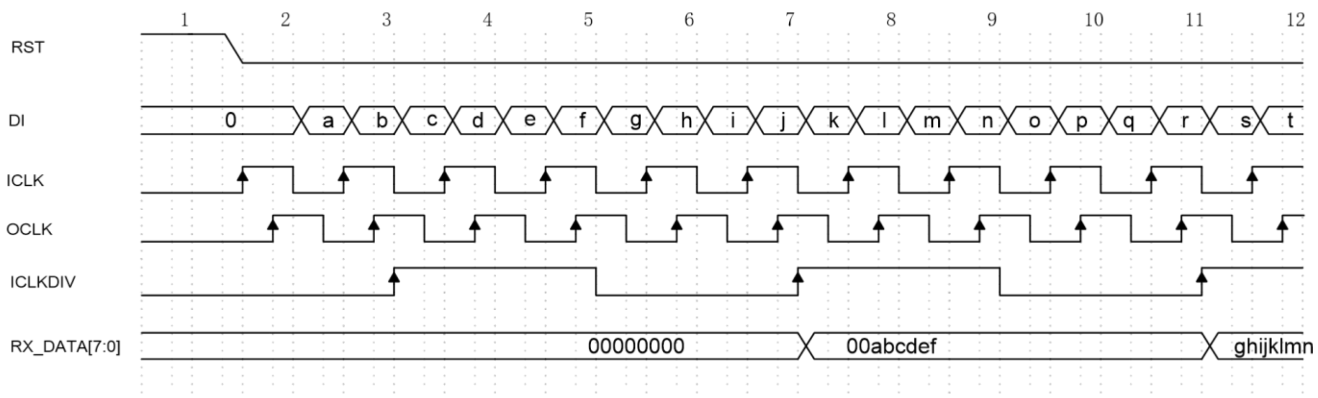


Figure 58 LMDDR1TO8 Timing Diagram

OVERSAMPLE

When the Input logic is configured as OVERSAMPLE mode, its function diagram can be simplified to the following diagram.

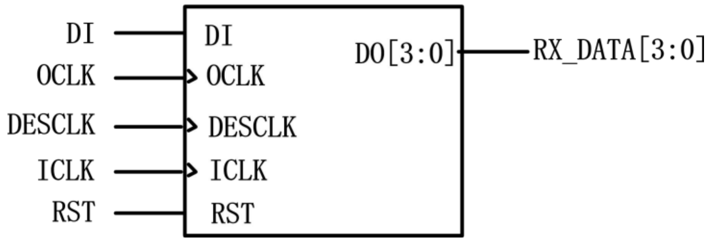


Figure 59 OVERSAMPLE Function Diagram

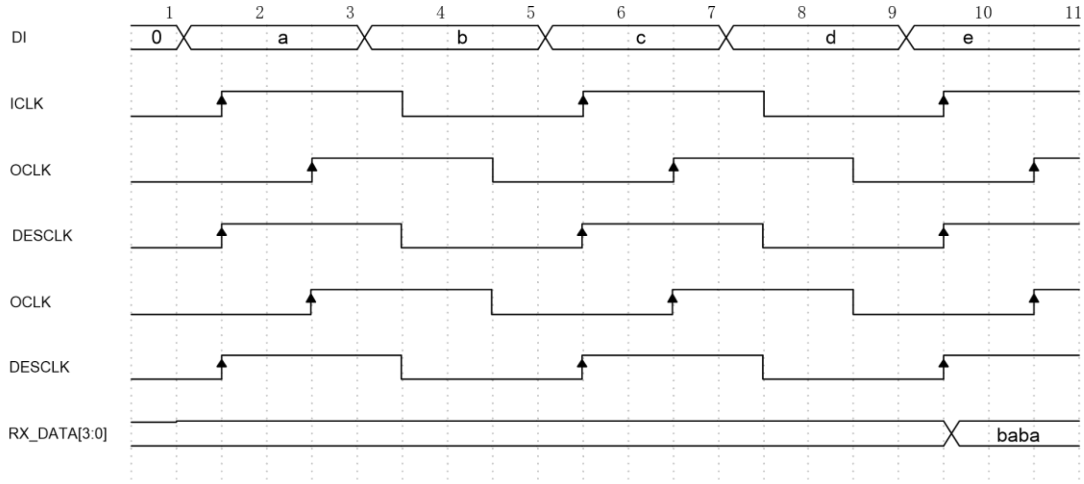


Figure 60 OVERSAMPLE Timing Diagram

As shown in the figure above, four clock signals with a phase difference of 90 degrees are used to sample the Input data di respectively, and the sampled result rx_data[3:0] is sent internally for further processing.

BITSLIP

In NETWORKING mode, the BITSLIP function is supported. The BITSLIP port must be kept valid for at least one ICLKDIV clock cycle. In SDR mode, two valid BITSLIP operations are separated by at least two ICLKDIV cycles. In DDR mode, two valid BITSLIP operations are separated by At least three ICLKDIV cycles.

In SDR mode, every time a BITSLIP request is generated, the original 1-bit data will be lost, so that the output data will be shifted to the left by 1 bit. As shown in Figure 61, when a bitslip request is generated, the original 1-bit data will be lost, and the output data will be shifted to the left by 1 bit. The output data changes from the original 00ab cdef ghij to 00ab defg hijk.

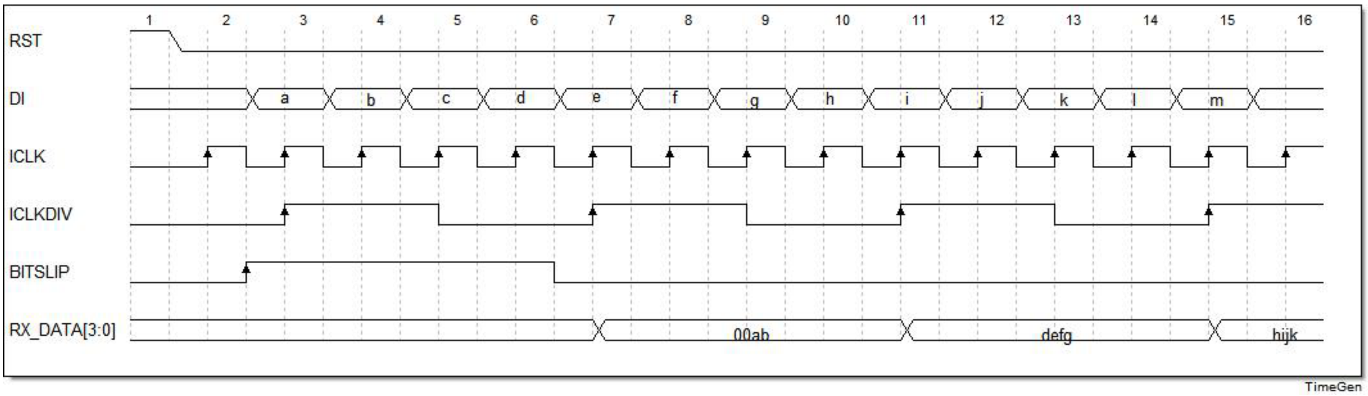


Figure 61 SDR1to4 with bitslip Timing Diagram

In DDR mode, when the odd-numbered BITSLIP request occurs, it is shifted to the right by 1 bit, and when the even-numbered BITSLIP request occurs, it is shifted to the left by 3 bits. But the difference between HR IOL and HP IOL is that HR IOL occurs when the odd-numbered BITSLIP request occurs, shift right by 1 bit, when an even-numbered BITSLIP request occurs, shift left by 3 bits. As shown in Figure 62, when the first bitslip request works, the output changes from efgh, ijkl, mnop, qrst to efgh, hijk, lmno, pqrs That is, the output data is shifted to the right by 1 bit; from the first bitslip request to the second bitslip request, the output changes from pqrs, tuvw, xyzA, BCDE to qprs, wxyz, ABCD, that is, the output data is shifted to the left by 3 bits. When the odd-numbered BITSLIP request occurs, the HP IOL shifts 1 bit to the right and loses 3 bits of data. When the even-numbered BITSLIP request occurs, it shifts 3 bits to the left and loses 7 bits of data. As shown in Figure 63, when the first bitslip request works, the output changes from ijkl, mnop, qrst to ijkl, pqrs, that is, the output data is shifted to the right by 1 bit, and 3 bits of data are lost; from the first bitslip request works, to the second bitslip request works, the output is from FGHI, JKLM, NOPQ, RSTU becomes FGHI, QRST means the output data is shifted to the left by 3 bits, and 7 bits of data are lost.

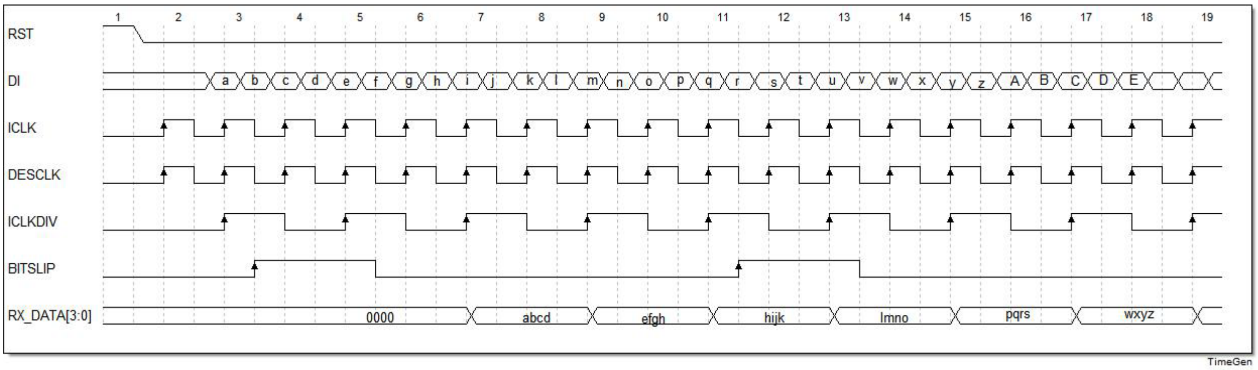


Figure 62 HR DDR1to4 with bitslip Timing Diagram

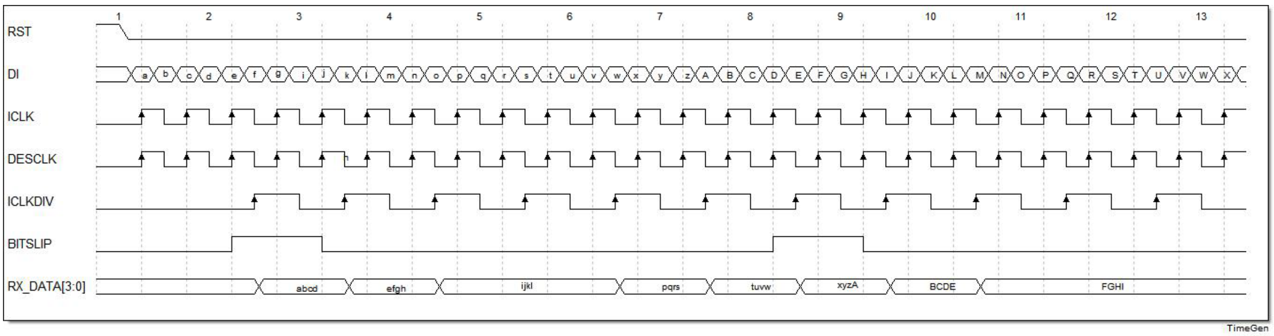


Figure 63 HP DDR1to4 with bitslip Timing Diagram

3. Output Logic

The output logic of the IOL is used to process the sent high-speed data and realize the conversion of high-speed parallel data into serial data. In order to realize the parallel-to-serial conversion function in the IOL, for HR BANK and HP BANK, PDS provides the GTP_OSERDES_E2 primitive, GTP_OSERDES_E2 data output conversion The module supports SDR2TO1, SDR3TO1, SDR4TO1, SDR5TO1, SDR6TO1, SDR7TO1, SDR8TO1, DDR2TO1_SAME_EDGE, DDR2TO1_OPPOSITE_EDGE, DDR4TO1, DDR6TO1, DDR8TO1, DDR10TO1, DDR14TO1, HMSDR2TO1, HMSDR4TO1, HMSDR8TO1, OLATCH, ODFF mode rate conversion. Its structural block diagram is as follows:

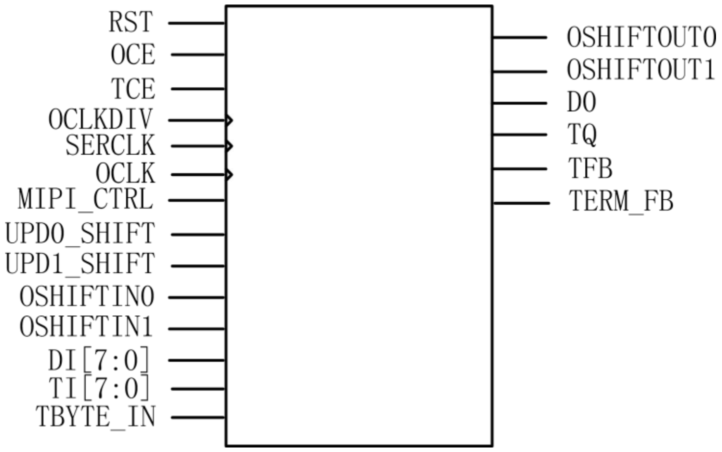


Figure 64 GTP_OSERDES_E2 Structure Diagram

The GTP_OSERDES_E2 Verilog instantiation is as follows:

```
GTP_OSERDES_E2 #(
.GRS_EN("TRUE"),
.OSERDES_MODE("SDR4TO1"),
.TSERDES_EN("FALSE"),
.UPD0_SHIFT_EN("FALSE"),
.UPD1_SHIFT_EN("FALSE"),
.INIT_SET('b00),
.GRS_TYPE_DQ("RESET"),
.LRS_TYPE_DQ0("ASYNC_RESET"),
.LRS_TYPE_DQ1("ASYNC_RESET"),
.LRS_TYPE_DQ2("ASYNC_RESET"),
.LRS_TYPE_DQ3("ASYNC_RESET"),
.GRS_TYPE_TQ("RESET"),
.LRS_TYPE_TQ0("ASYNC_RESET"),
.LRS_TYPE_TQ1("ASYNC_RESET"),
.LRS_TYPE_TQ2("ASYNC_RESET"),
.LRS_TYPE_TQ3("ASYNC_RESET"),
.TRI_EN("FALSE"),
.TBYTE_EN("FALSE"),
.MIPI_EN("FALSE"),
.OCASCADE_EN("FALSE"),
.HPIO("FALSE"),
.ODELAY_EN("FALSE"),
.TDELAY_EN("FALSE"),
.TSERDES_MODE("SDR4TO1"),
.TUPD0_SHIFT_EN("FALSE"),
.TUPD1_SHIFT_EN("FALSE"),
.TINIT_SET('b00),
.TERMBYTE_EN("FALSE"),
.TERM_EN("FALSE"),
.TERM_OFF_SET('b00),
.TERM_ON_SET('b00)
) <InstanceName> (
.DI(DI),
```

```
    .TI(TI),
    .DO(DO),
    .OSHIFTOUT0(OSHIFTOUT0),
    .OSHIFTOUT1(OSHIFTOUT1),
    .TERM_FB(TERM_FB),
    .TFB(TFB),
    .TQ(TQ),
    .MIPI_CTRL(MIPI_CTRL),
    .OCE(OCE),
    .OCLK(OCLK),
    .OCLKDIV(OCLKDIV),
    .OSHIFTIN0(OSHIFTIN0),
    .OSHIFTIN1(OSHIFTIN1),
    .RST(RST),
    .SERCLK(SERCLK),
    .TBYTE_IN(TBYTE_IN),
    .TCE(TCE),
    .UPD0_SHIFT(UPD0_SHIFT),
    .UPD1_SHIFT(UPD1_SHIFT)
    );
```

It is worth noting that GTP_OSERDES_E2 is only used as OSERDES mode, and the parameter TSERDES_EN of GTP_OSERDES_E2 needs to be set to "FLASE".

When OSERDES and TSERDES are used together, GTP_OSERDES_E2 needs to be instantiated twice, one of which sets the GTP_OSERDES_E2 parameter TSERDES_EN to "FLASE" as OSERDES, and the other GTP_OSERDES_E2 parameter TSERDES_EN is set to "TRUE" as TSERDES, and TSERDES is used to generate three-state control Signal, to process the data signal generated by OSERDES.

For high-speed output applications, when OSERDES is SDR 2TO1, TSERDES is SDR 2TO1; when OSERDES is SDR 4TO1, TSERDES is SDR 4TO1; when OSERDES is SDR 8TO1, TSERDES is SDR 8TO1; when OSERDES is DDR 4TO1, TSERDES is DDR 4TO1; OSERDES When it is DDR 8TO1, TSERDES is DDR 8TO1. For MEMORY applications, when OSERDES is SDR 4TO1, TSERDES is SDR 4TO1; when OSERDES is SDR 8TO1, TSERDES is SDR 8TO1; other modes do not support the use of OSERDES and TSERDES.

GTP_OSERDES_E2 cannot be set alone for TSERDES use.

GTP_OSERDES_E2 is usually used together with GTP_OUTBUF, GTP_OUTBUFDS, GTP_OUTBUFCO, GTP_OUTBUFTCO, GTP_OUTBUFTDS and GTP_OUTBUFT.

Table 53 GTP_OSERDES_E2 parameter description

Name	Type	Settings	Defaults	Functional description
HPIO	String	"TRUE", "FALSE"	"FALSE"	TRUE for OSERDES using HPIO, otherwise HRIO
ODELAY_EN	String	"TRUE", "FALSE"	"FALSE"	TRUE indicates that the output MUX data source uses ODELAY
TDELAY_EN	String	"TRUE", "FALSE"	"FALSE"	TRUE indicates that the output MUX data source uses TDELAY

Name	Type	Settings	Defaults	Functional description
OSERDES_MODE	String	"SDR2TO1" "SDR3TO1" "SDR4TO1" "SDR5TO1" "SDR6TO1" "SDR7TO1" "SDR8TO1" "OLATCH" "ODFF" "DDR2TO1_SAME_ EDGE" "DDR2TO1_OPPOSITE_ EDGE" "DDR4TO1" "DDR6TO1" DDR8TO1" "DDR10TO1" "DDR14TO1" "HMSDR4TO1" "HMSDR8TO1"	SDR4TO1	"SDR2TO1": Generic SDR 2:1 serialization mode "SDR3TO1": Generic SDR 3:1 serialization mode "SDR4TO1": Generic SDR 4:1 serialization mode "SDR5TO1": Generic SDR 5:1 serialization mode "SDR6TO1": Generic SDR 6:1 serialization mode "SDR7TO1": Generic SDR 7:1 serialization mode "SDR8TO1": Generic SDR 8:1 serialization mode "OLATCH": Latch output mode "ODFF" register output mode "DDR2TO1_SAME_EDGE": Generic DDR 2:1 serialization mode "DDR2TO1_OPPOSITE_EDGE": Generic DDR 2:1 serialization mode "DDR4TO1": Generic DDR 4:1 serialization mode "DDR6TO1": Generic DDR 6:1 serialization mode "DDR8TO1": Generic DDR 8:1 serialization mode "DDR10TO1": Generic DDR 10:1 serialization mode "DDR14TO1": Generic DDR 14:1 serialization mode "HMSDR4TO1": High-Speed Memory SDR 4:1 serialization mode "HMSDR8TO1": High-Speed Memory SDR 8:1 serialization mode
TSERDES_MODE	String	"SDR2TO1" "SDR4TO1" "SDR8TO1" "TLATCH" "TDFF" "DDR2TO1_SAME_EDGE" "DDR2TO1_OPPOSITE_ EDGE" "DDR4TO1" "DDR8TO1" "HMSDR4TO1" "HMSDR8TO1"	SDR4TO1	"SDR2TO1": Generic SDR 2:1 serialization mode "SDR4TO1": Generic SDR 4:1 serialization mode "SDR8TO1": Generic SDR 8:1 serialization mode "TLATCH": Latch output mode "TDFF" register output mode "DDR2TO1_SAME_EDGE": Generic DDR 2:1 serialization mode "DDR2TO1_OPPOSITE_EDGE": Generic DDR 2:1 serialization mode "DDR4TO1": Generic DDR 4:1 serialization mode "DDR8TO1": Generic DDR 8:1 serialization mode "HMSDR4TO1": High-Speed Memory DDR 4:1 serialization mode "HMSDR8TO1": High-Speed Memory DDR 8:1 serialization mode
UPD0_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	upd0 position control enable in OLOGIC
UPD1_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	upd1 position control enable in OLOGIC
TUPD0_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	upd0 position control enable in TSERDES
TUPD1_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	upd1 position control enable in TSERDES

Name	Type	Settings	Defaults	Functional description
INIT_SET[1:0]	Constance	2'b00, 2'b01, 2'b10, 2'b11	2'b00	Static control of upd0, upd1 position in OSERDES 2'b00: default position; 2'b01: move forward by one period; 2'b10: move forward two periods; 2'b11: move forward three periods;
TINIT_SET[1:0]	Constance	2'b00, 2'b01, 2'b10, 2'b11	2'b00	Static control of upd0, upd1 position in TSERDES 2'b00: default position; 2'b01: move forward by one period; 2'b10: move forward two periods; 2'b11: move forward three periods;
LRS_TYPE_DQ2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF2 local reset/set result in OLOGIC data gear;
LRS_TYPE_DQ3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF3 local reset/set result in OLOGIC data gear;
GRS_TYPE_TQ	String	"RESET" "SET"	"RESET"	Global reset results of DFF0, DFF1, DFF2, DFF3, DFF4 in OLOGIC tri-state gear;
LRS_TYPE_TQ0	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF0 local reset/set result in OLOGIC tri-state gear;
LRS_TYPE_TQ1	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF1 local reset/set result in OLOGIC tri-state gear;
LRS_TYPE_TQ2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF2 local reset/set result in OLOGIC tri-state gear;
LRS_TYPE_TQ3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	DFF3 local reset/set result in OLOGIC tri-state gear;
TSERDES_EN	String	"FALSE" "TRUE"	"FALSE"	TSERDES enable *Note: When oserdes and tserdes are used together, TSERDES_EN = "FALSE" of oserdes; TSERDES_EN = "TRUE" of tserdes; when only using oserdes, TSERDES_EN = "FALSE"
TRI_EN	String	"FALSE" "TRUE"	"FALSE"	Tri-state control enable IOLHR: *Note: When oserdes and tserdes are used together, TRI_EN="TRUE" of oserdes; TRI_EN="FALSE" of tserdes; when only using oserdes, enable the tri-state function TRI_EN="TRUE", disable the tri-state function TRI_EN="FALSE".

Name	Type	Settings	Defaults	Functional description
				IOLHP: Turn on when using TSERDES, TRI_EN="TRUE"; turn off when not using, TRI_EN="FALSE";
TBYTE_EN	String	"FALSE" "TRUE"	"FALSE"	BYTE control enable *Note: When oserdes and tserdes are used together, TBYTE_EN="TRUE" for oserdes, TBYTE_EN="FALSE" for tserdes
TERMBYTE_EN	String	"FALSE" "TRUE"	"FALSE"	TERM BYTE control enable
OCASCADE_EN	String	"FALSE" "TRUE"	"FALSE"	OSERDES extension enable
TERM_EN	String	"FALSE" "TRUE"	"FALSE"	Terminal control signal TERM enable
TERM_OFF_SET	Constance	2'b00, 2'b01, 2’b10, 2'b11	2'b00	TERM signal off (falling edge) bias 2'b00: synchronized with the tri-state signal; 2'b01: advance to TI data update; 2'b10: advance to UPD0 valid; 2'b11: advance to UPD1 valid;
TERM_ON_SET	Constance	2'b00, 2'b01, 2’b10, 2'b11	2'b00	TERM signal on (rising edge) bias 2'b00: synchronized with the tri-state signal; 2'b01: delay one cycle; 2'b10: delay two cycles; 2'b11: delay three cycles;

Table 54 GTP_OSERDES_E2 port description

Port Signal	Input/Output	Width	Description
RST	Input	1	Local reset signal (need to be valid for at least two OCLKDIV clock cycles), active high
OCE	Input	1	Output module clock enable signal
TCE	Input	1	Tri-state module clock enable signal
OCLKDIV	Input	1	OLOGIC low-speed clock (OCLKDIV and SERCLK are synchronous clocks)
SERCLK	Input	1	OLOGIC serialized clock
OCLK	Input	1	OLOGIC output stage high speed clock
MIPI_CTRL	Input	1	Output mipi (low speed/high speed) control signal
UPD0_SHIFT	Input	1	OLOGIC's UPD0 location move
UPD1_SHIFT	Input	1	OLOGIC's UPD1 location move
OSHIFTIN0	Input	1	Cascading Input Signals

Port Signal	Input/Output	Width	Description
OSHIFTIN1	Input	1	Cascading Input Signals
DI	Input	8	Parallel Input data signal
TI	Input	2	Parallel Input tri-state control signal
TBYTE_IN	Input	1	Can control a byte tri-state control Input signal
OSHIFTOUT0	Output	1	Cascading Input Signals
OSHIFTOUT1	Output	1	Cascading Input Signals
DO	Output	1	data output
TQ	Output	1	Three-state control output (to IOB)
TFB	Output	1	Three-state control output (to internal logic)
TERM_FB	Output	1	Terminal control output (to internal logic)

Direct Output

The following describes the output logic configuration as direct output mode, which is divided into register output and latch output.

ODFF

When the output logic is configured in ODFF mode, its functional diagram can be simplified as the following figure.



Figure 65 ODFF Function Diagram

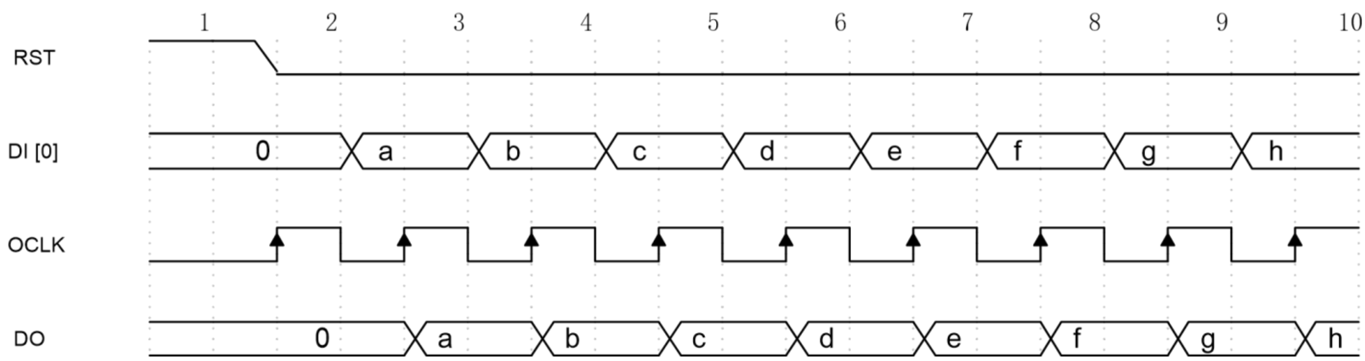


Figure 66 ODFF Timing Diagram

OLATCH

When the output logic is configured as OLATCH mode, its function diagram can be simplified as the following diagram.



Figure 67 OLATCH Function Diagram

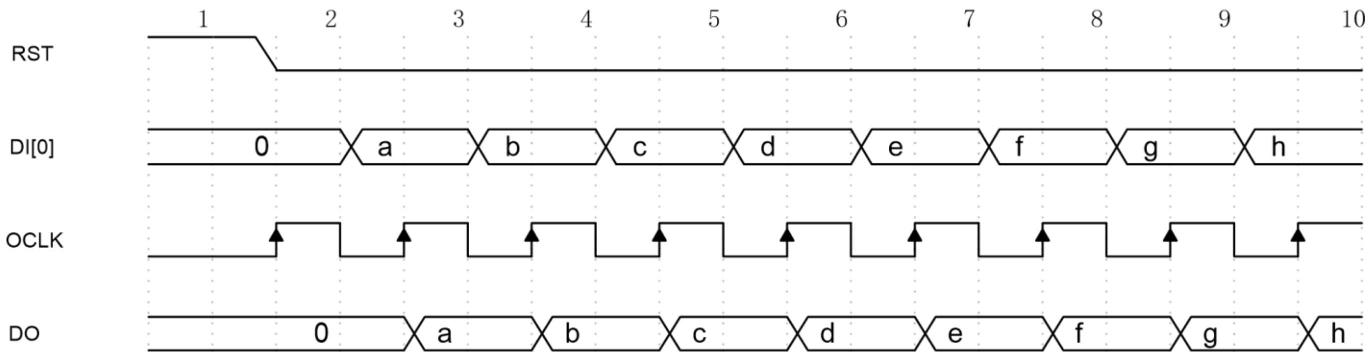


Figure 68 OLATCH Timing Diagram

ODDR

GTP_ODDR_E1 is a data parallel-to-serial processing module that supports SAME_EDGE and OPPOSITE_EDGE modes, and its structural block diagram is shown below.

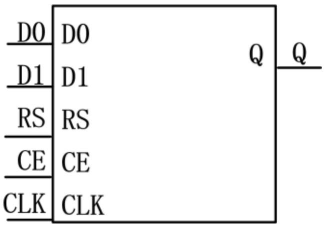


Figure 69 GTP_ODDR_E1 Structure Diagram

Table 55 Port description of GTP_ODDR_E1

Port Signal	Input/Output	Width	Description
D0	Input	1	Data input
D1	Input	1	Data input
CE	Input	1	Clock enable
RS	Input	1	Set/reset
CLK	Input	1	System clock
Q	Output	1	Data output

Table 56 GTP_ODDR_E1 parameter list description

Name	Type	Settings	Defaults	Functional description
ODDR_MODE	string	"SAME_EDGE" "OPPOSITE_EDGE"	"SAME_EDGE"	"SAME_EDGE": DDR 2:1 serialization mode "OPPOSITE_EDGE": DDR 2:1 serialization mode
GRS_EN	string	"FALSE" "TRUE"	"TRUE"	Global reset enable
RS_TYPE	string	"SYNC_SET" "ASYNC_SET" "SYNC_RESET" "ASYNC_RESET"	"ASYNC_RESET"	Reset/Set Mode Selection: Synchronous Set, Asynchronous Set, Synchronous Reset, Asynchronous Reset

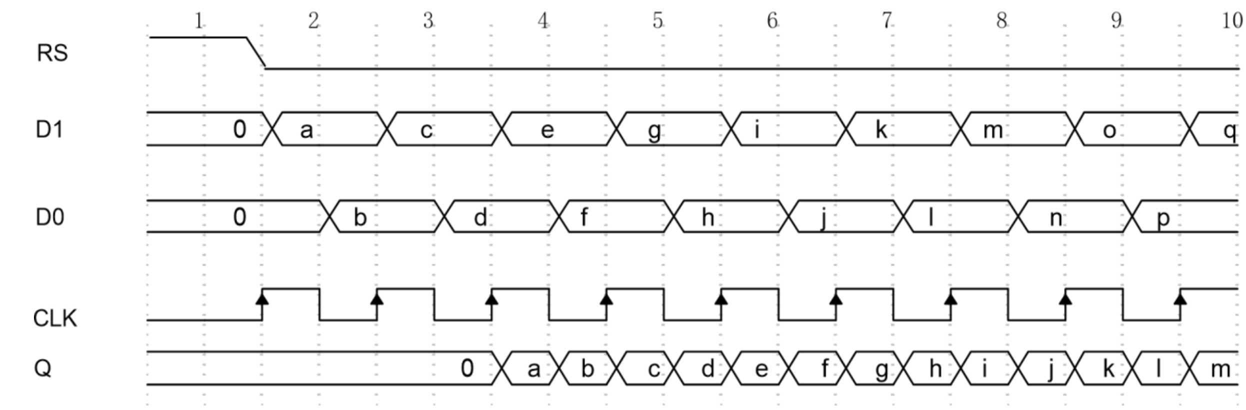


Figure 70 GTP_ODDR_E1 OPPOSITE_EDGE Mode Timing Diagram

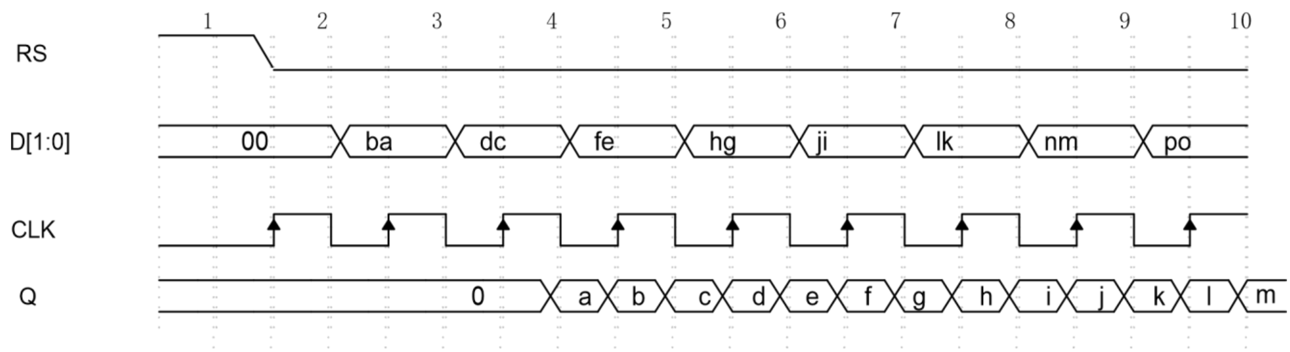


Figure 71 GTP_ODDR_E1 SAME_EDGE Mode Timing Diagram

OSERDES

The following describes the different operating modes in which the output logic is configured as OSERDES.

SDR2TO1

When the Input logic is configured as SDR2TO1 mode, its function diagram can be simplified as the following diagram.

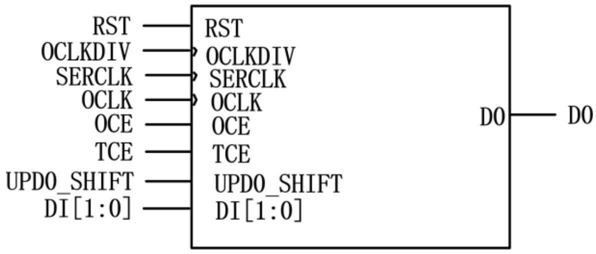


Figure 72 SDR2TO1 Function Diagram

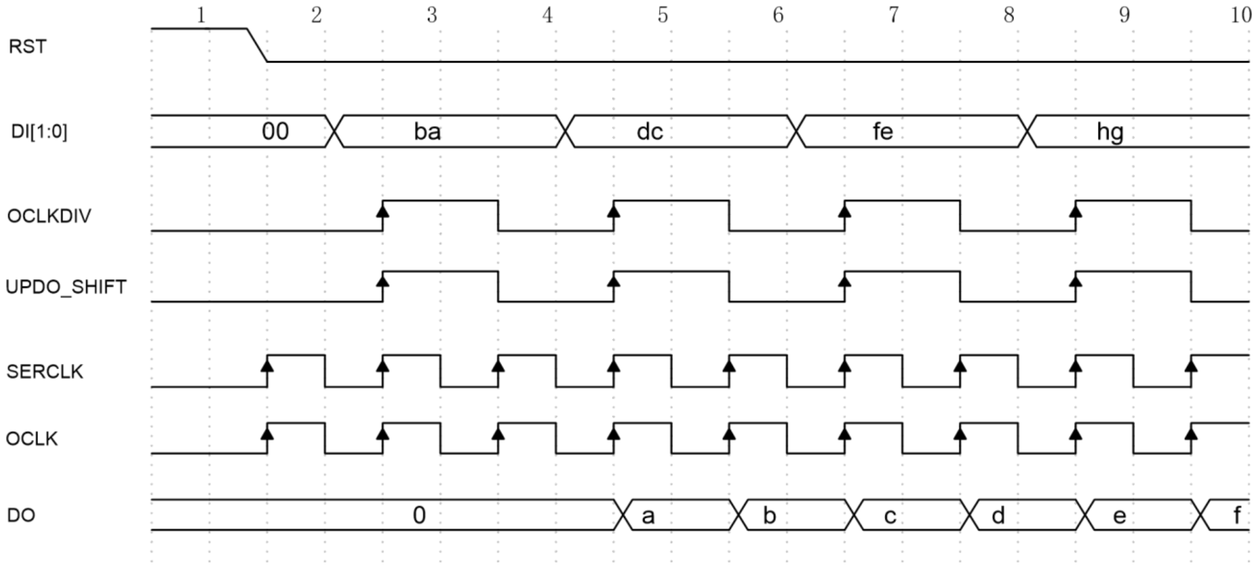


Figure 73 SDR2TO1 Timing Diagram

SDR3TO1

When the output logic is configured as SDR3TO1 mode, its functional diagram can be simplified as the following figure.

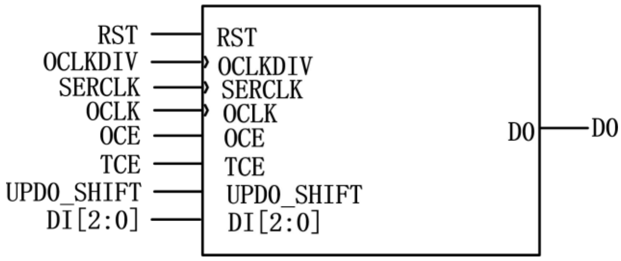


Figure 74 SDR3TO1 Function Diagram

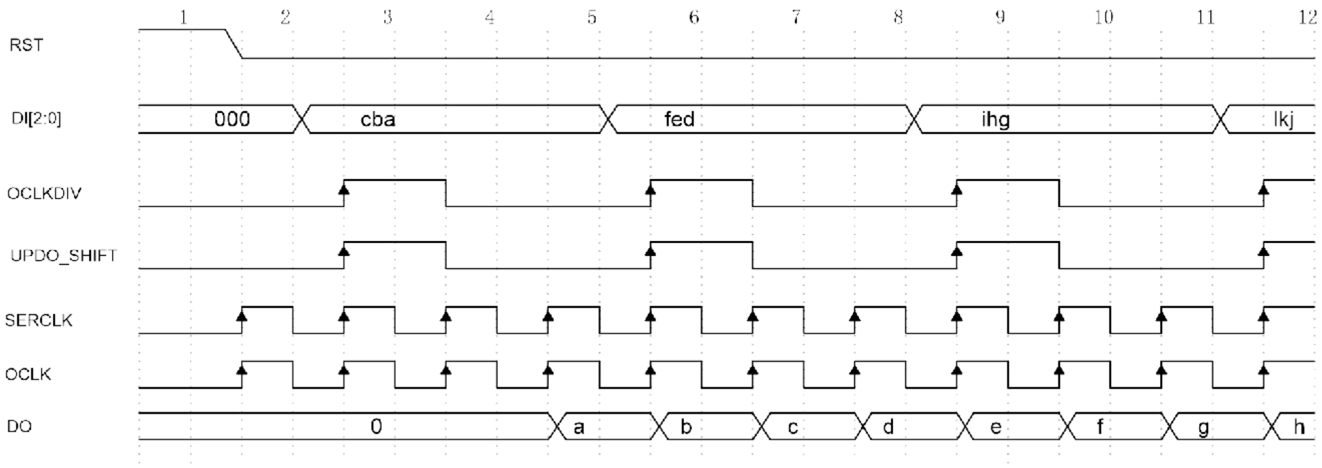


Figure 75 SDR3TO1 Timing Diagram

SDR4TO1

When the output logic is configured as SDR4TO1 mode, its functional diagram can be simplified to the following figure.

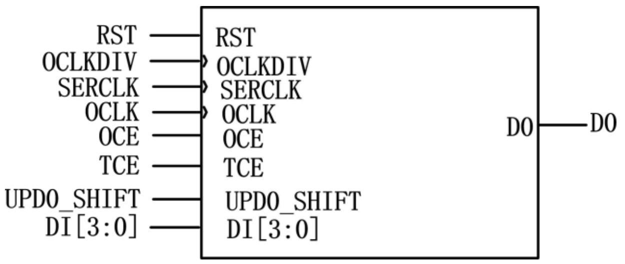


Figure 76 SDR4TO1 Function Diagram

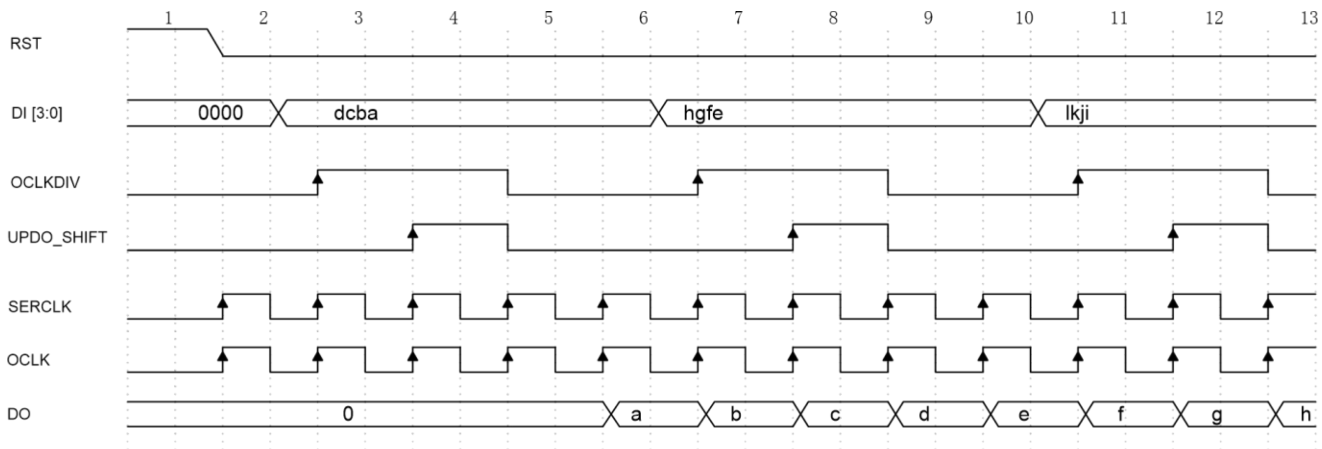


Figure 77 SDR4TO1 Timing Diagram

SDR5TO1

When the output logic is configured as SDR5TO1 mode, its functional diagram can be simplified to the following figure.

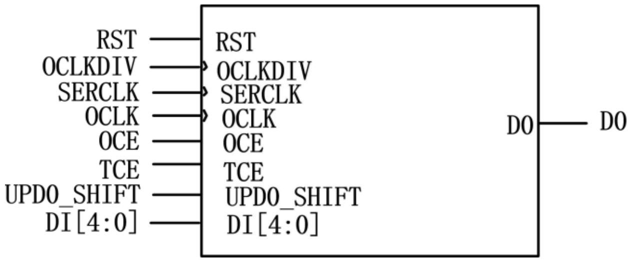


Figure 78 SDR5TO1 Function Diagram

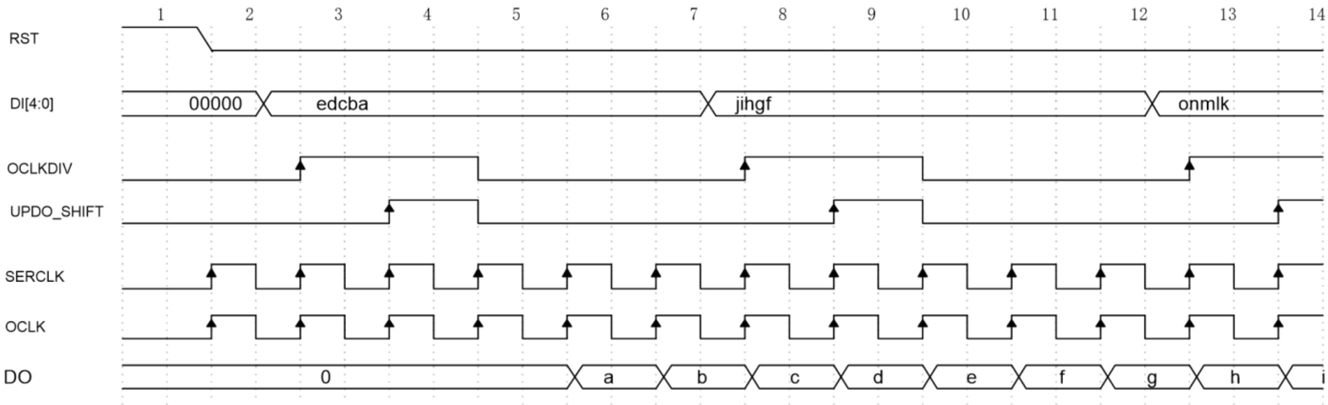


Figure 79 SDR5TO1 Timing Diagram

SDR6TO1

When the output logic is configured as SDR6TO1 mode, its functional diagram can be simplified to the following figure.

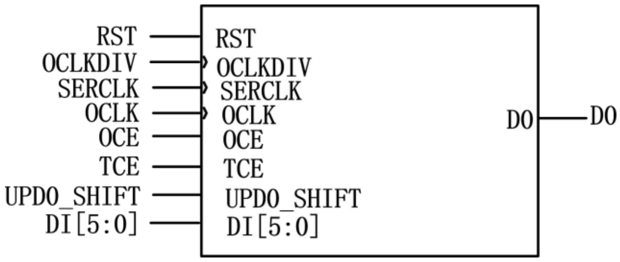


Figure 80 SDR6TO1 Function Diagram

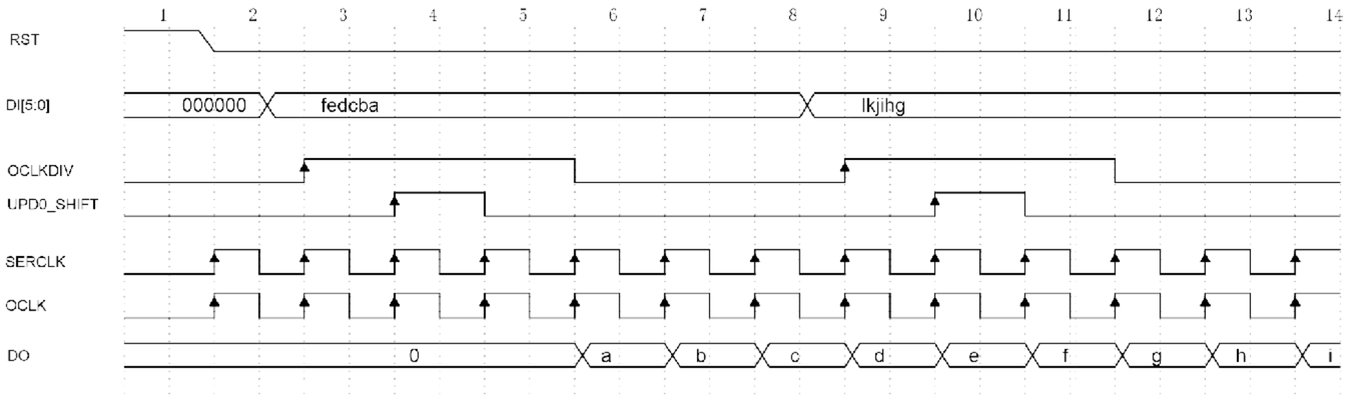


Figure 81 SDR6TO1 Timing Diagram

SDR7TO1

When the output logic is configured as SDR7TO1 mode, its functional diagram can be simplified to the following figure.

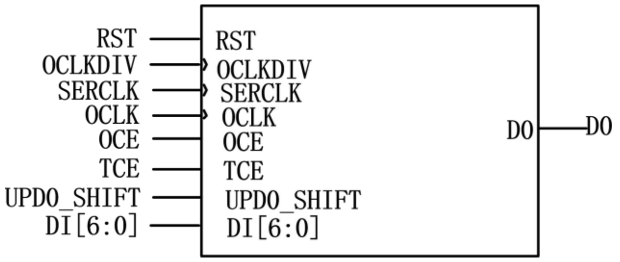


Figure 82 SDR7TO1 Function Diagram

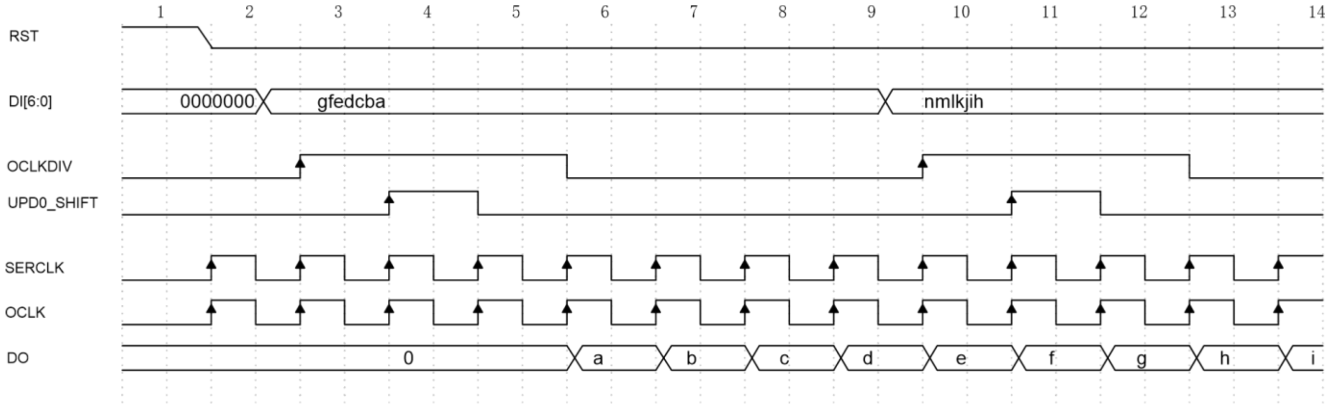


Figure 83 SDR7TO1 Timing Diagram

SDR8TO1

When the output logic is configured as SDR8TO1 mode, its functional diagram can be simplified as the following figure.

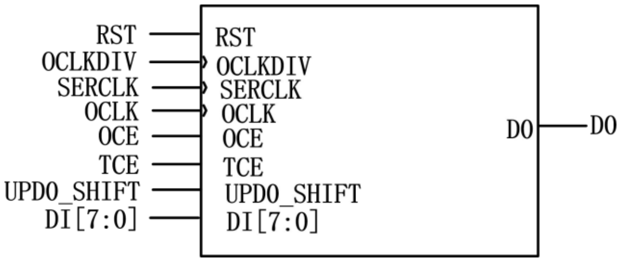


Figure 84 SDR8TO1 Function Diagram

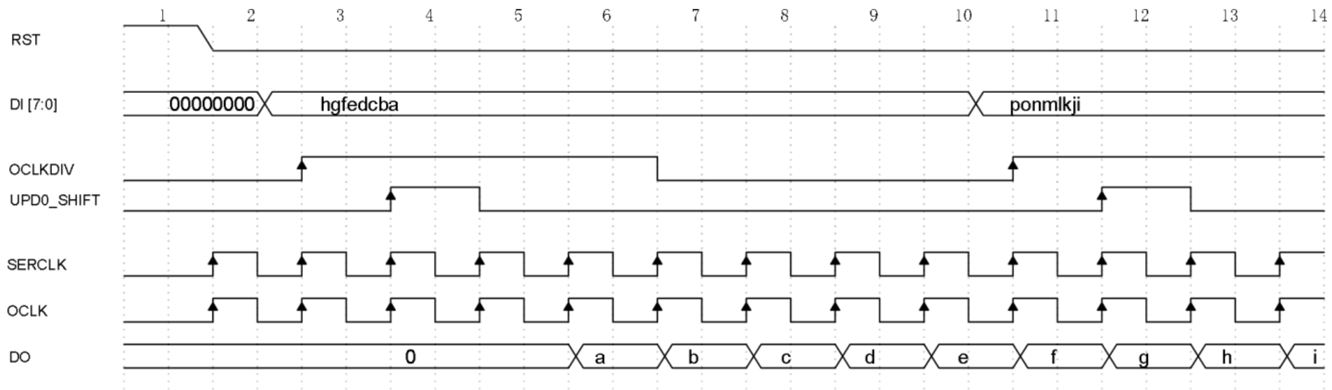


Figure 85 SDR8TO1 Timing Diagram

DDR2TO1_OPPOSITE_EDGE

When the output logic is configured as DDR2TO1_OPPOSITE_EDGE mode, its functional diagram can be simplified as the following figure.

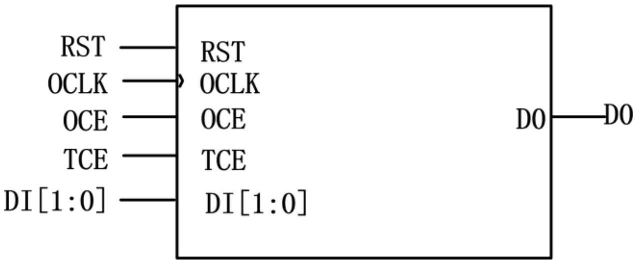


Figure 86 DDR2TO1_OPPOSITE_EDGE Function Diagram

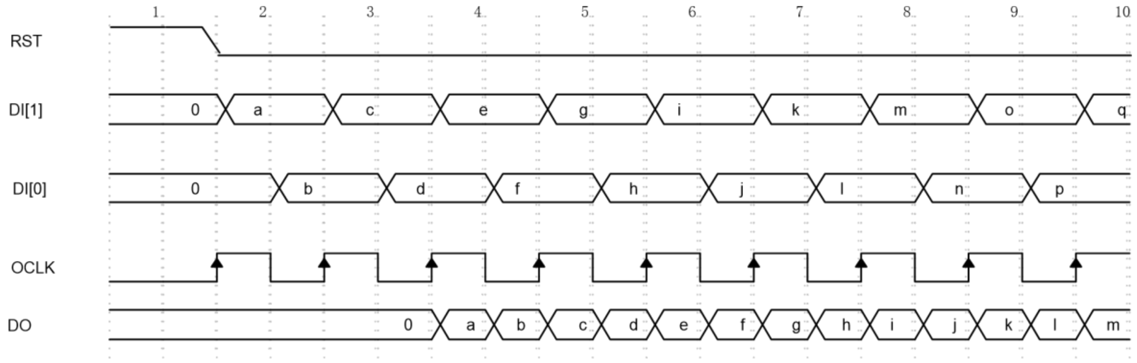


Figure 87 DDR2TO1_OPPOSITE_EDGE Timing Diagram

DDR2TO1_SAME_EDGE

When the output logic is configured as DDR2TO1_SAME_EDGE mode, its functional diagram can be simplified as the following figure.

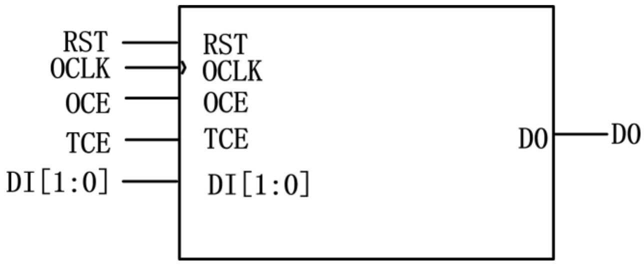


Figure 88 DDR2TO1_SAME_EDGE Function Diagram

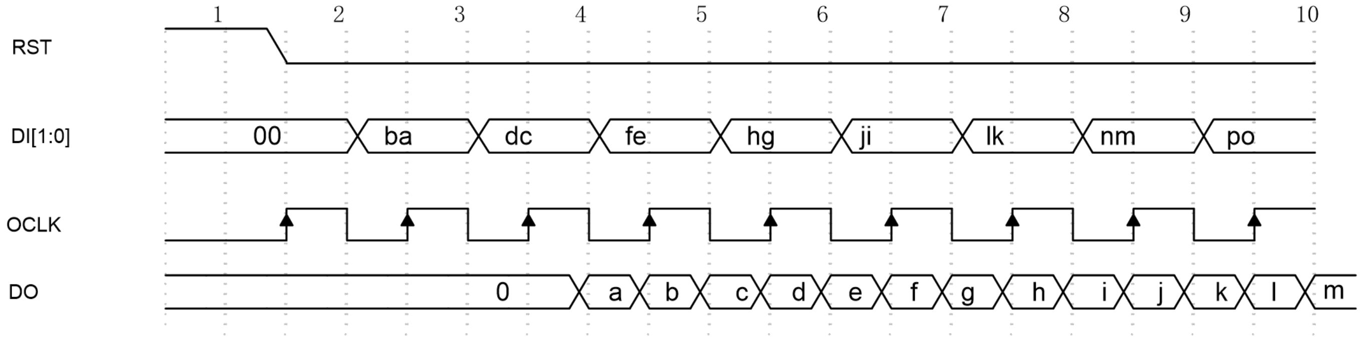


Figure 89 DDR2TO1_SAME_EDGE Timing Diagram

DDR4TO1

When the output logic is configured as DDR4TO1 mode, its functional diagram can be simplified as the following figure.

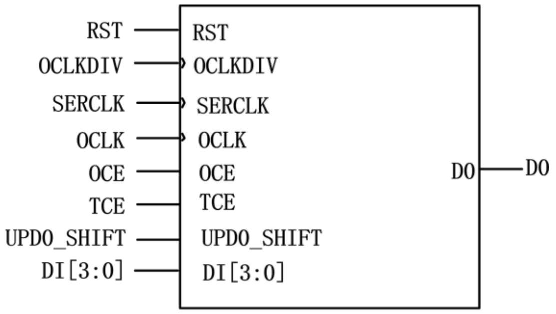


Figure 90 DDR4TO1 Function Diagram

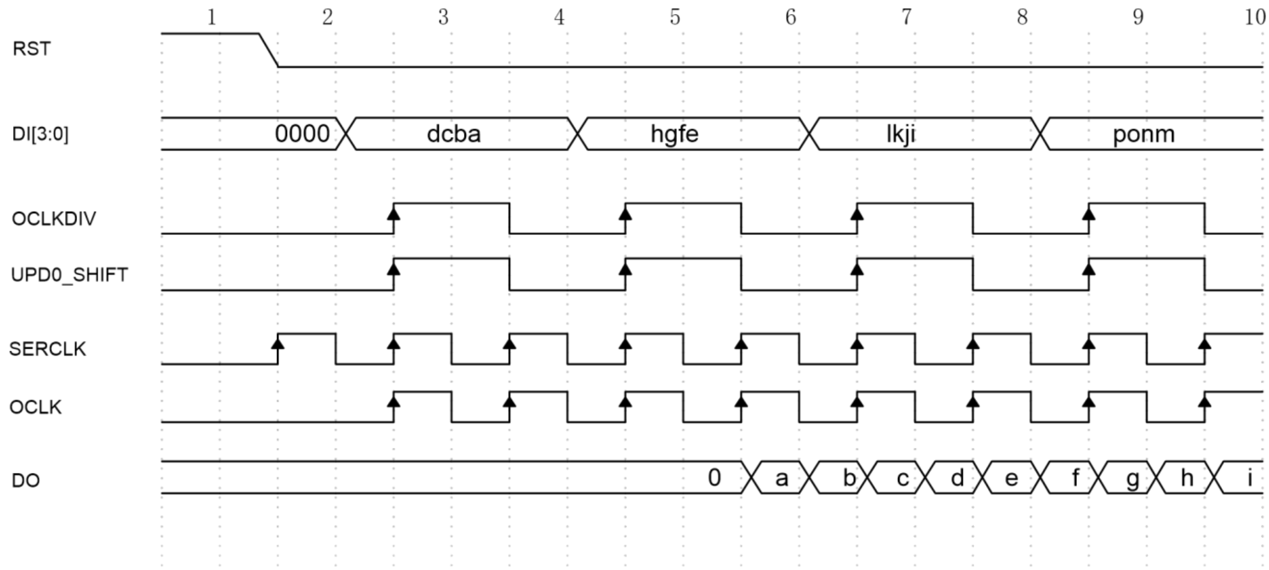


Figure 91 DDR4TO1 Timing Diagram

DDR6TO1

When the output logic is configured as DDR6TO1 mode, its functional diagram can be simplified to the following figure.

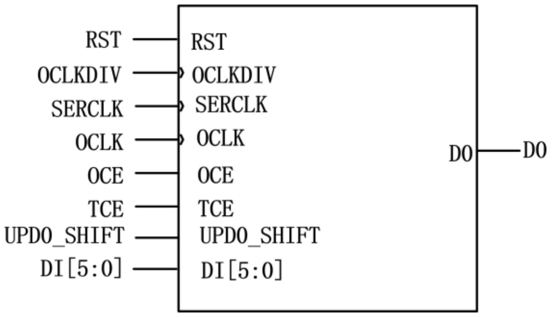


Figure 92 DDR6TO1 Function Diagram

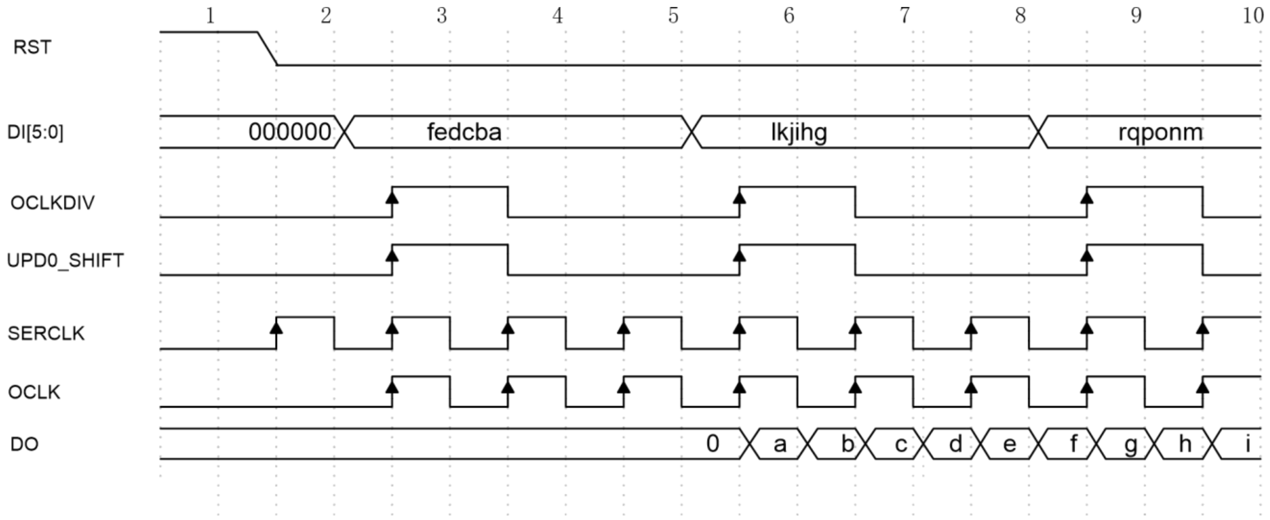


Figure 93 DDR6TO1 Timing Diagram

DDR8TO1

When the output logic is configured as DDR8TO1 mode, its functional diagram can be simplified to the following figure.

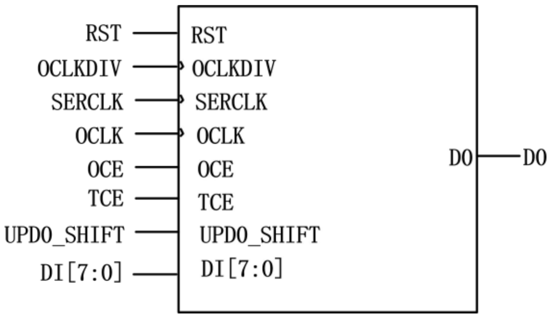


Figure 94 DDR8TO1 Function Diagram

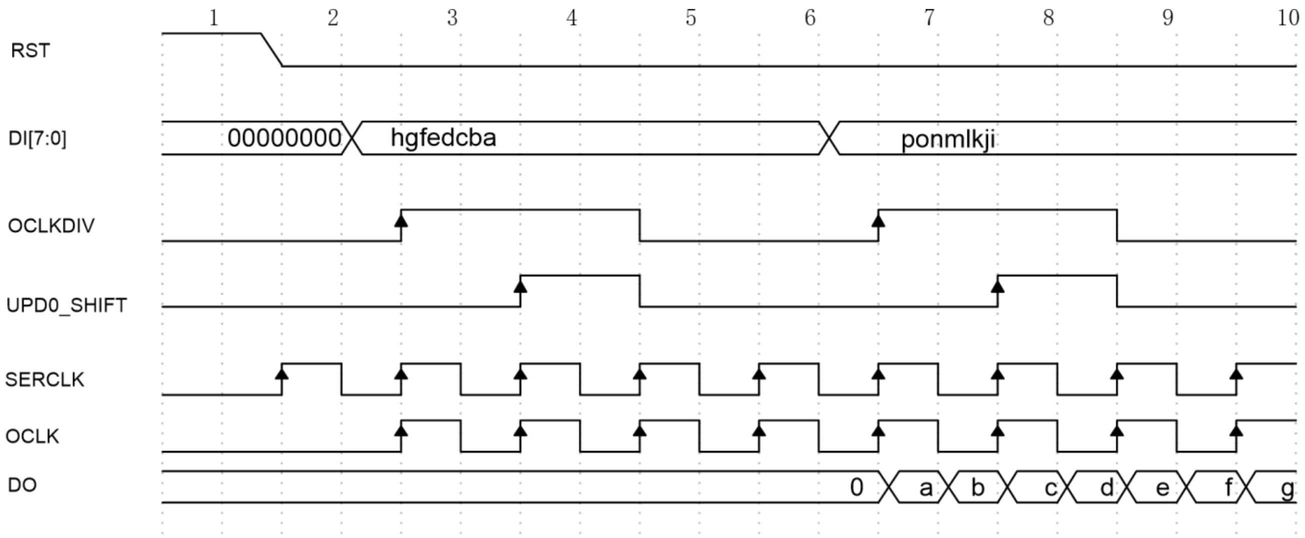


Figure 95 DDR8TO1 Timing Diagram

DDR10TO1

When the output logic is configured as DDR10TO1 mode, its functional diagram can be simplified to the following figure.

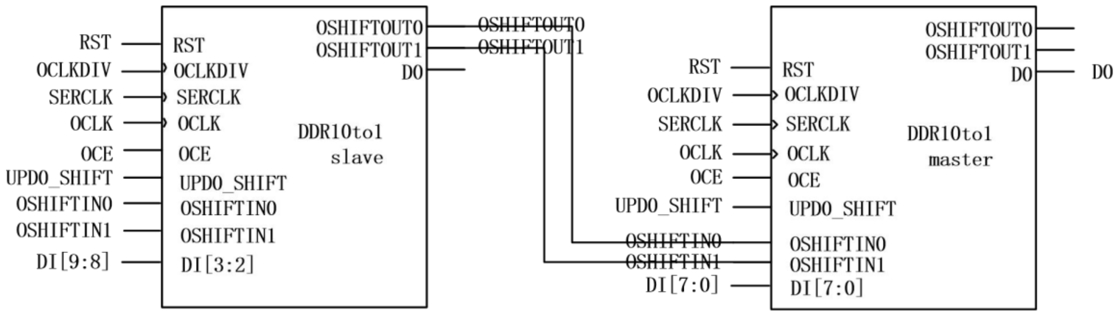


Figure 96 DDR10TO1 Function Diagram

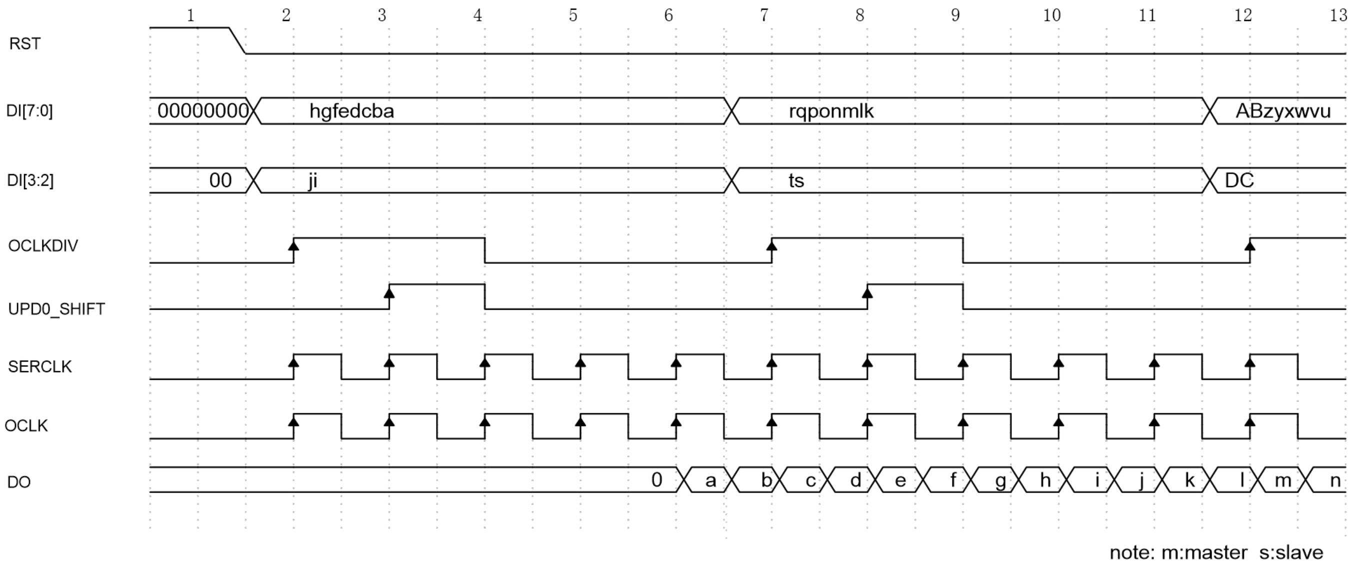


Figure 97 DDR10TO1 Timing Diagram

DDR14TO1

When the output logic is configured as DDR14TO1 mode, its functional diagram can be simplified as the following figure.

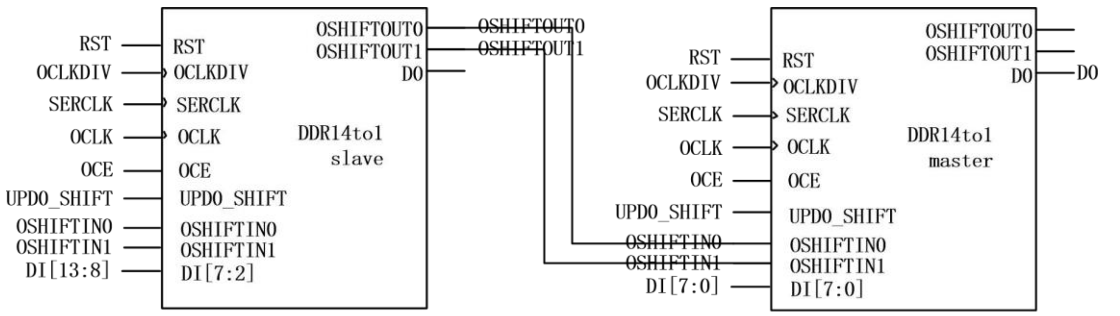


Figure 98 DDR14TO1 Function Diagram

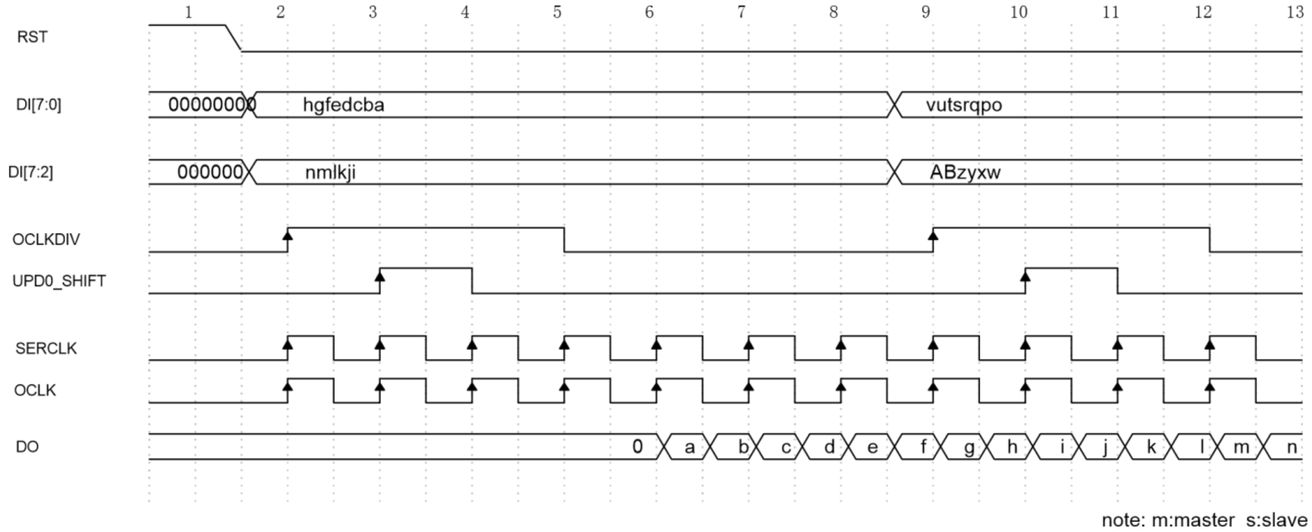


Figure 99 DDR14TO1 Timing Diagram

HMSDR4TO1

When the output logic is configured as HMSDR4TO1 mode, its functional diagram can be simplified to the following figure.

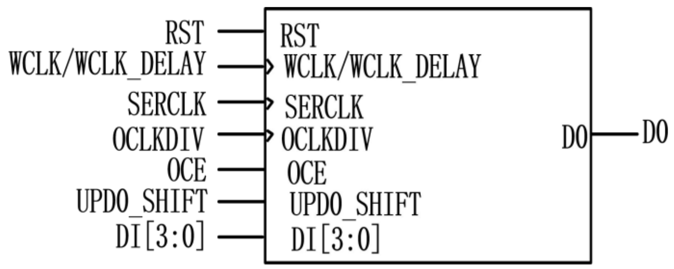


Figure 100 HMSDR4TO1 Function Diagram

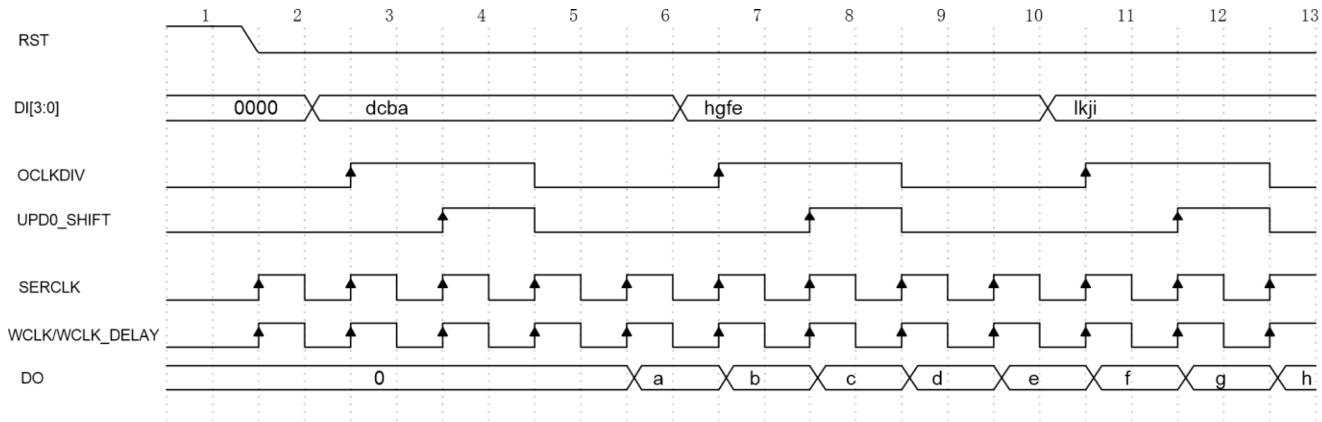


Figure 101 HMSDR4TO1 Timing Diagram

HMSDR8TO1

When the output logic is configured as HMSDR8TO1 mode, its functional diagram can be simplified to the following figure.

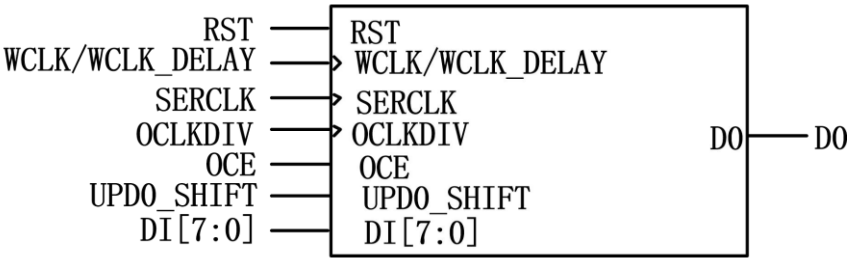


Figure 102 HMSDR8TO1 Function Diagram

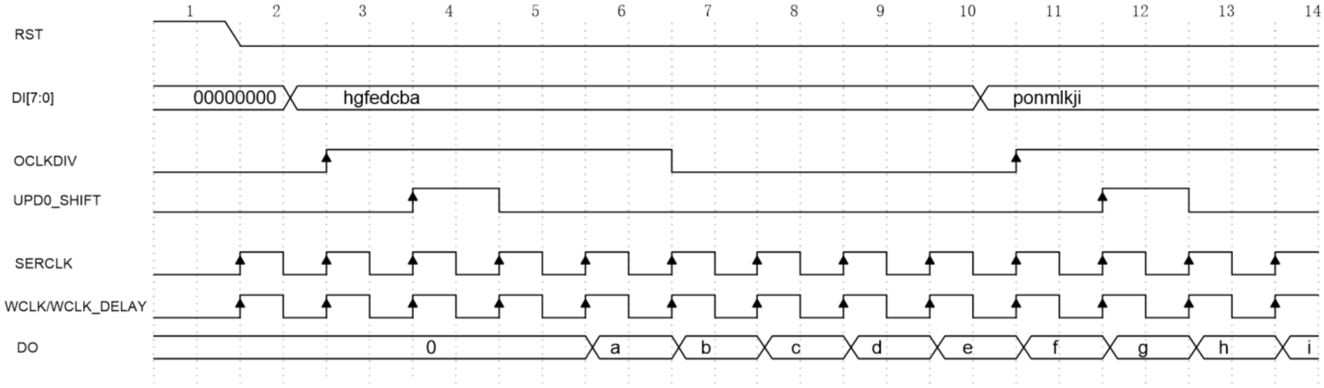


Figure 103 HMSDR8TO1 Timing Diagram

TSERDES

When OSERDES and TSERDES are used together, the output logic is set to TSERDES, and there are several different working modes as follows.

SDR2TO1

When the Input logic is configured as SDR2TO1 mode, its connection diagram can be simplified as the following figure.

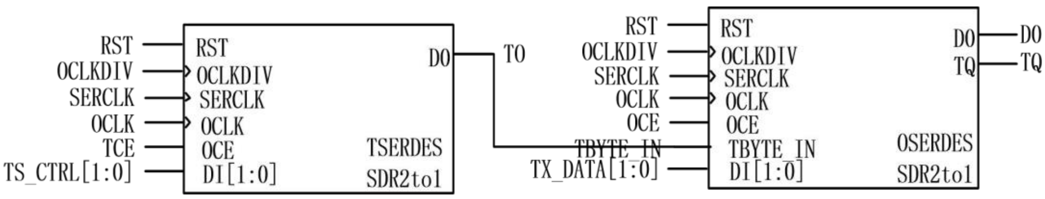


Figure 104 TSERDES SDR2TO1 Connection Diagram

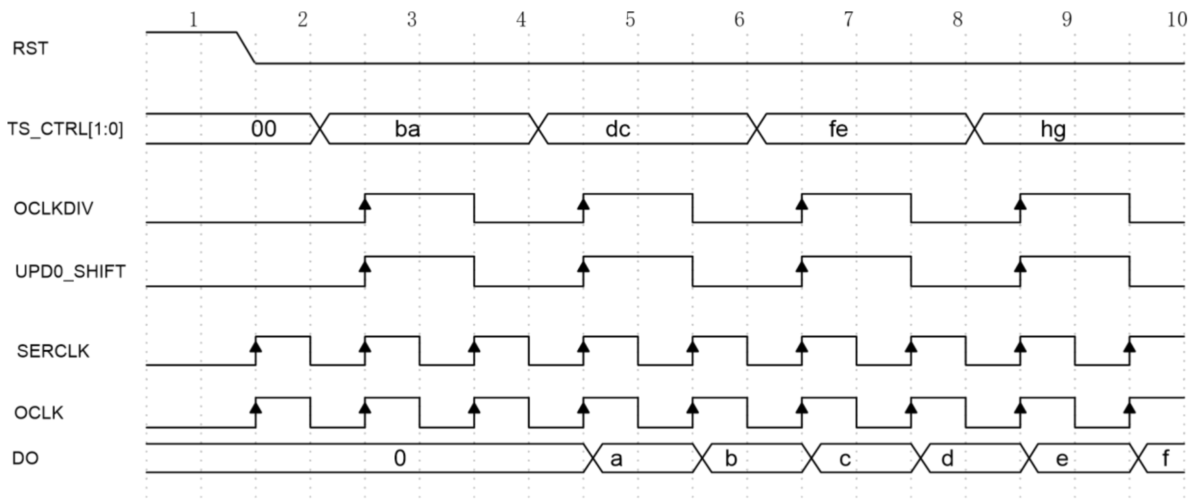


Figure 105 TSERDES SDR2TO1 Timing Diagram

SDR4TO1

When the output logic is configured as SDR4TO1 mode, its connection diagram can be simplified as the following figure.

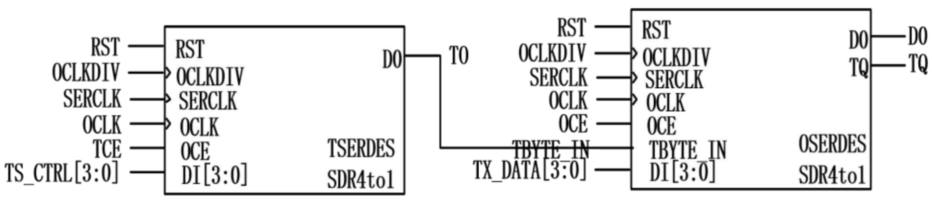


Figure 106 TSERDES SDR4TO1 Connection Diagram

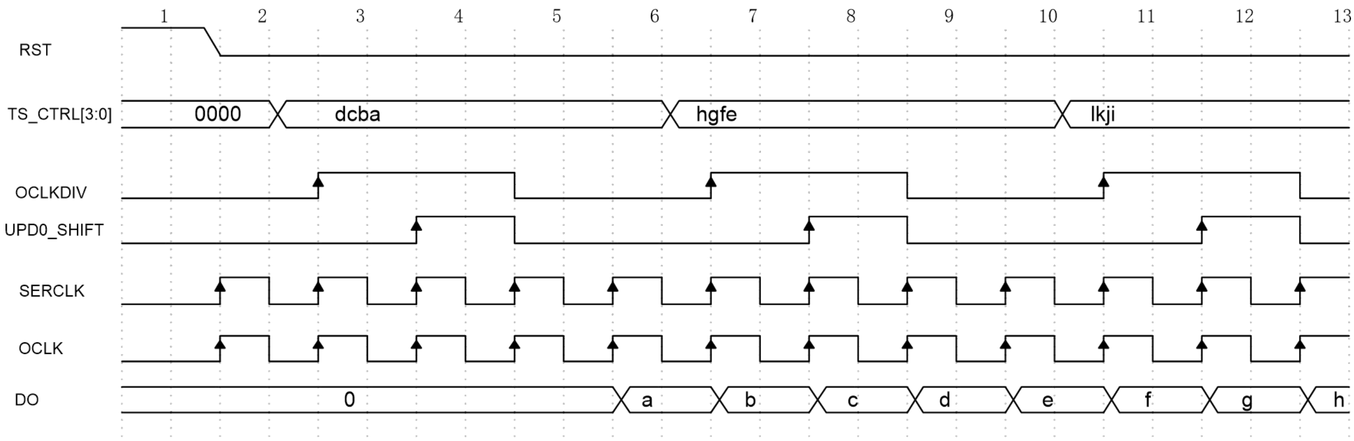


Figure 107 TSERDES SDR4TO1 Timing Diagram

SDR8TO1

When the output logic is configured as SDR8TO1 mode, its connection diagram can be simplified as the following figure.

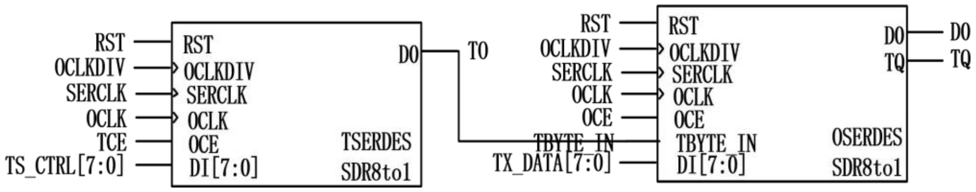


Figure 108 TSERDES SDR8TO1 Connection Diagram

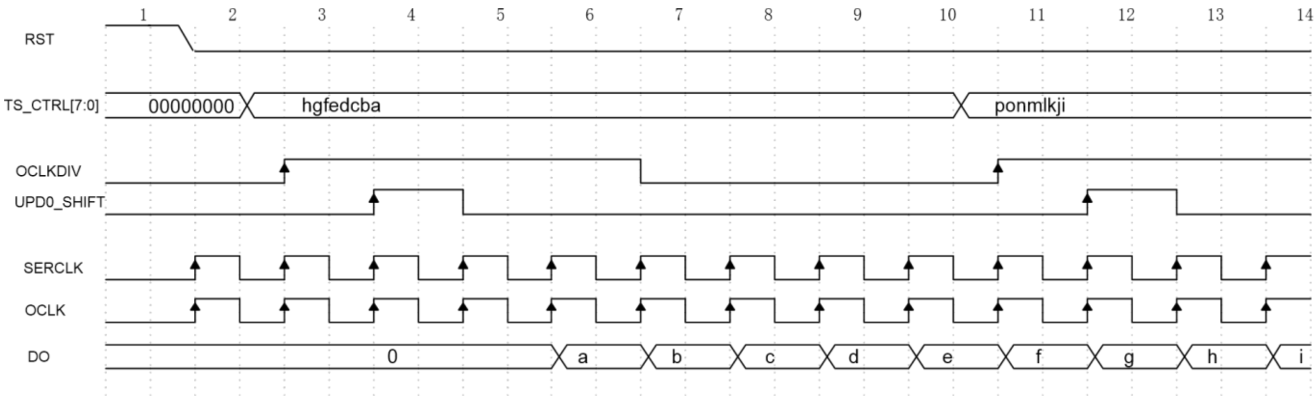


Figure 109 TSERDES SDR8TO1 Timing Diagram

DDR4TO1

When the output logic is configured as DDR4TO1 mode, its connection diagram can be simplified as the following figure.

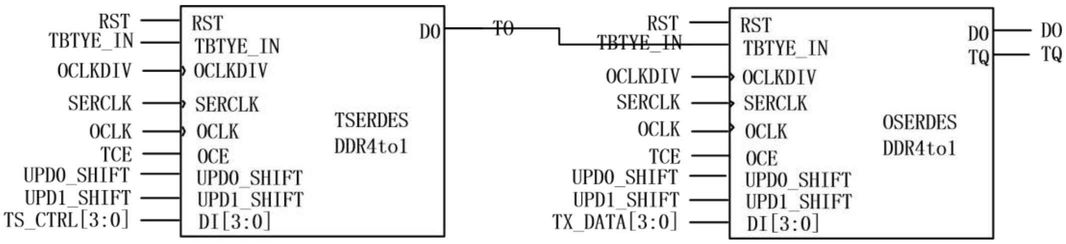


Figure 110 TSERDES DDR4TO1 Connection Diagram

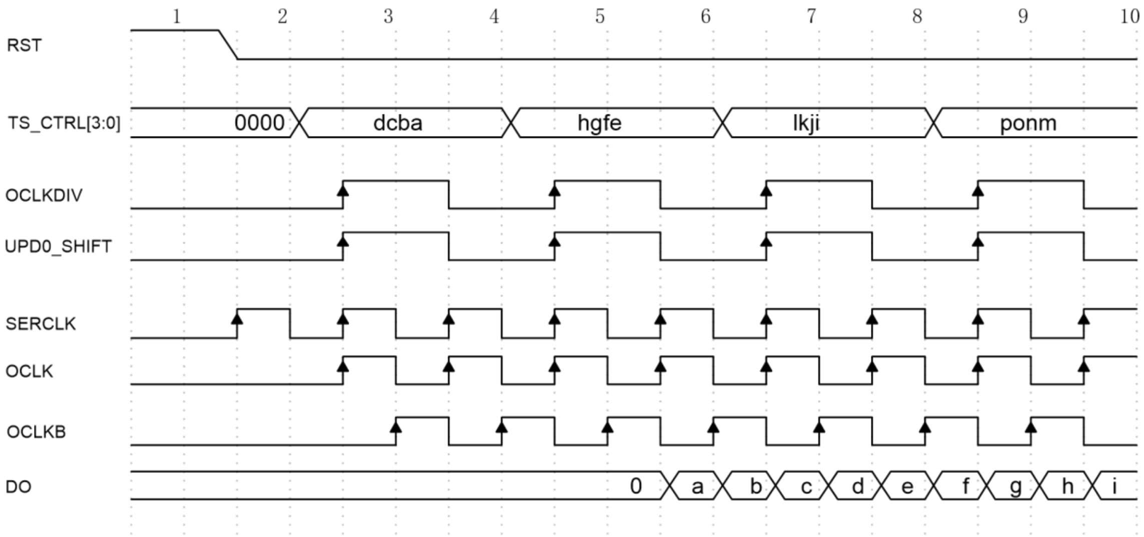


Figure 111 TSERDES DDR4TO1 Timing Diagram

DDR8TO1

When the output logic is configured as DDR8TO1 mode, its connection diagram can be simplified as the following figure.

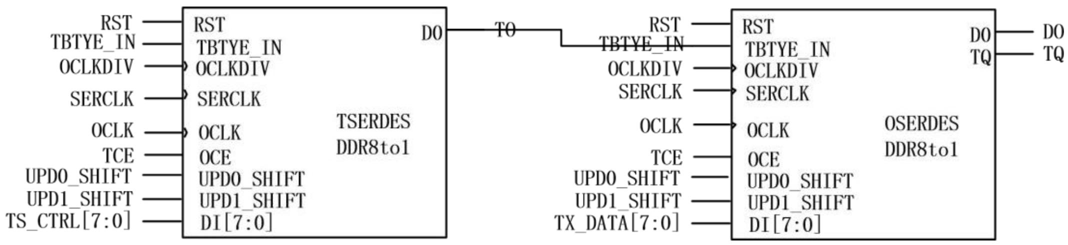


Figure 112 TSERDES DDR8TO1 Connection Diagram

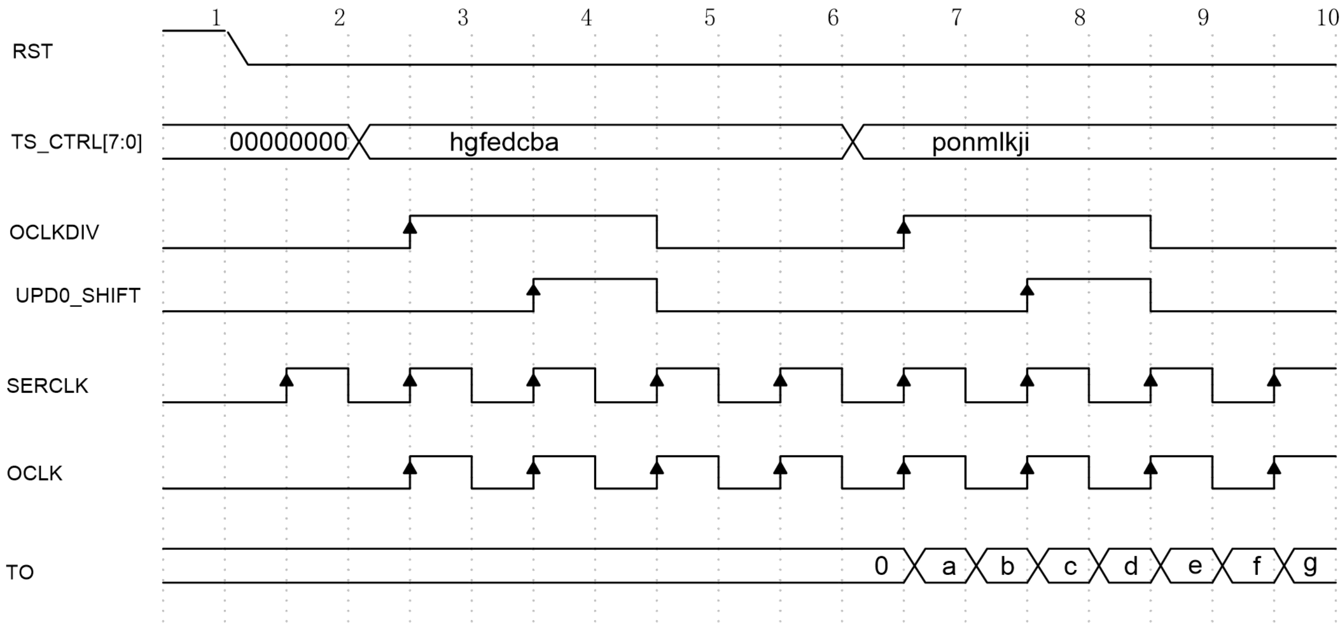


Figure 113 TSERDES DDR8TO1 Function Diagram

HMSDR4TO1

When the output logic is configured as HMSDR4TO1 mode, its connection diagram can be simplified as the following figure.

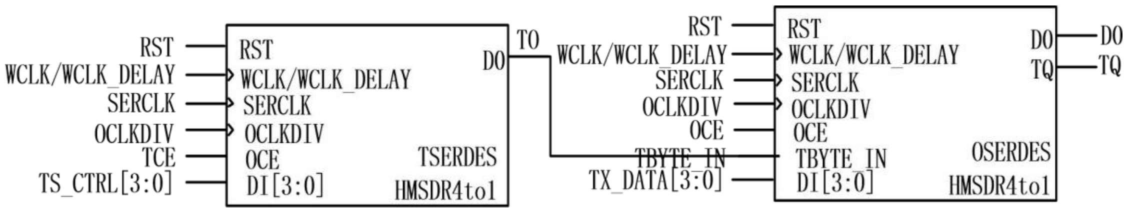


Figure 114 TSERDES HMSDR4TO1 Connection Diagram

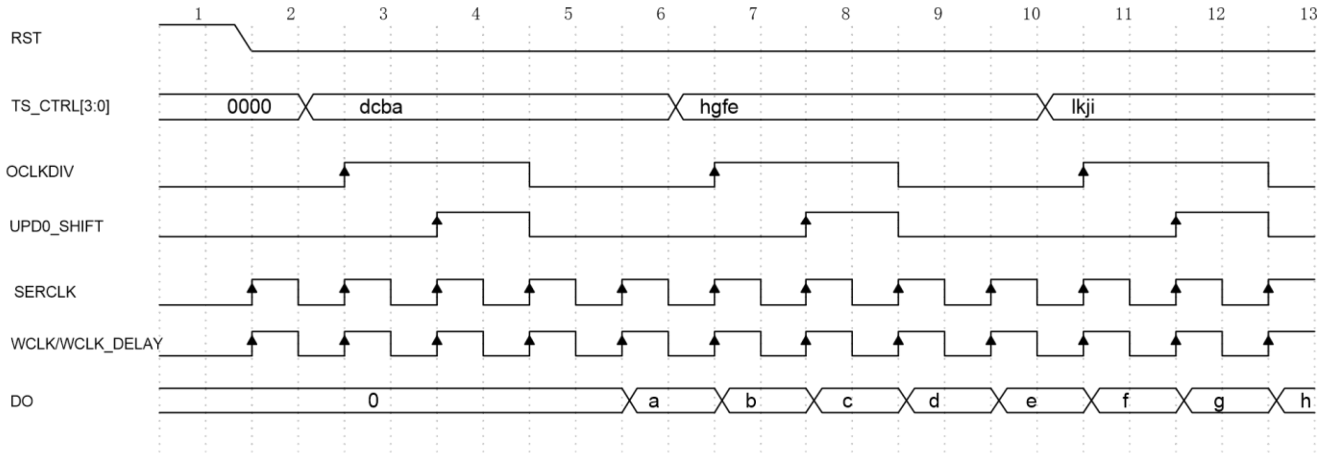


Figure 115 TSERDES HMSDR4TO1 Timing Diagram

HMSDR8TO1

When the output logic is configured as HMSDR8TO1 mode, its connection diagram can be simplified as the following figure.

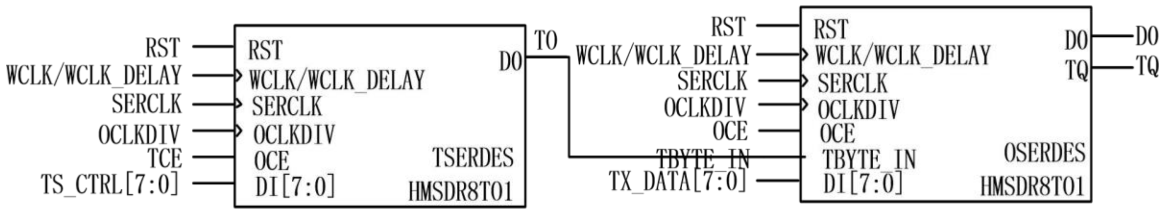


Figure 116 TSERDES HMSDR8TO1 Connection Diagram

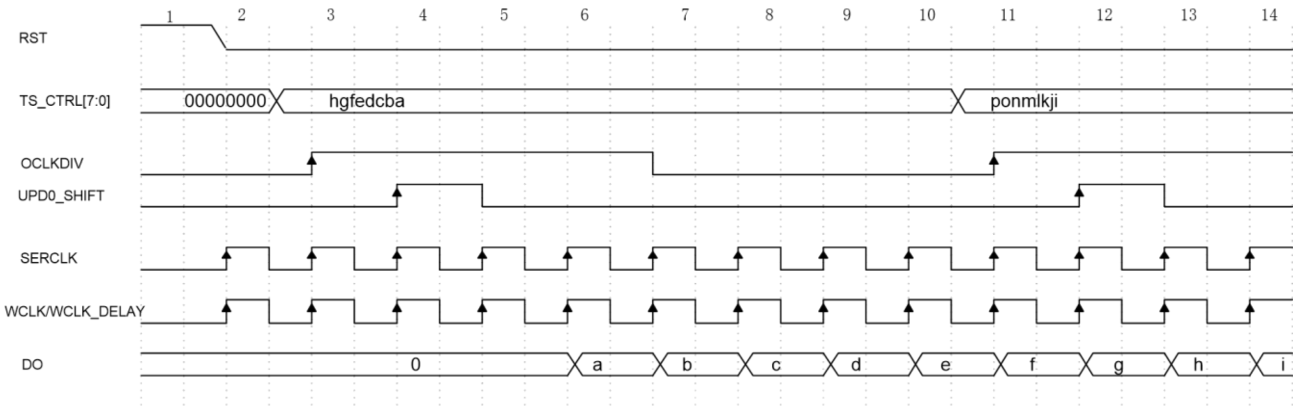


Figure 117 TSERDES HMSDR8TO1 Timing Diagram

4. Software setting input and output registers

The way to use the Input output register is to check under "IO_REGISTER" of the corresponding IO in PDS>UCE>Device>I/O Tabs, as shown in the figure below.

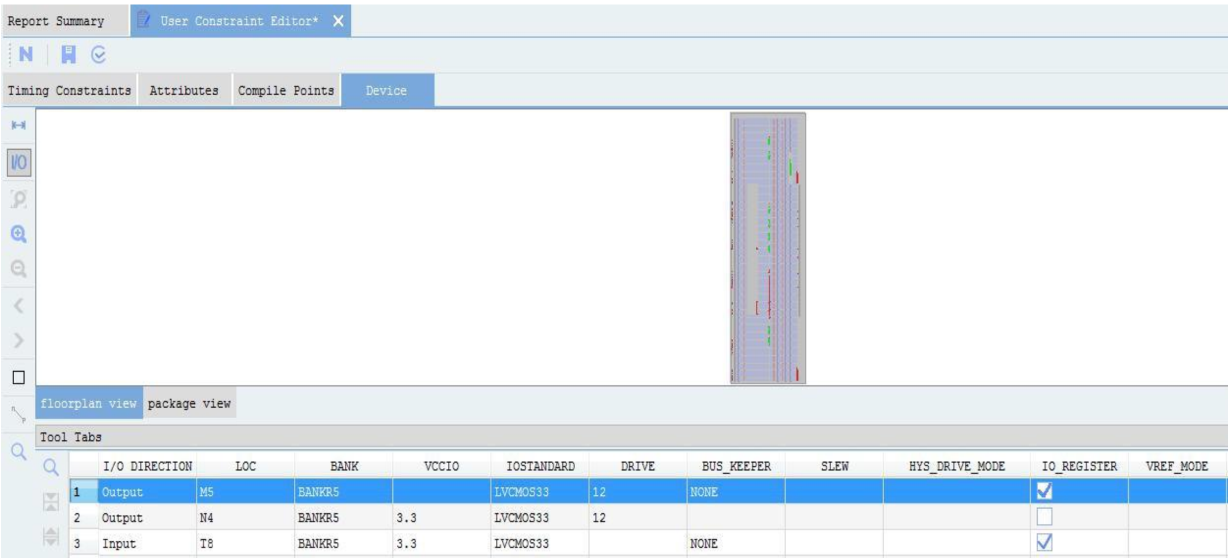


Figure 118 Schematic diagram of IO register constraint method

Disclaimers

Copyright Notice

Disclaimers

1. This document only provides phased information, and the content contained in it can be updated at any time according to the actual situation of the product without prior notice. The company does not assume any legal responsibility for any direct or indirect losses caused by improper use of this document.

2. This document is provided as is, without any warranty of any kind, including any warranties of merchantability, fitness for a particular purpose, or non-infringement, and any warranty of any proposal, specification or sample mentioned elsewhere. No license, express or implied, to any intellectual property right is hereby granted by estoppel or otherwise.

3. The company reserves the right to modify the relevant documents of the company's series of products at any time without prior notice.

Замечания по переводу отправляйте в ЛС пользователю Zig сайта electronix.ru